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Department of Physics

APPLIED PHYSICS - I

18K3CSAP1

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UNIT-IV: BOOLEAN ALGEBRA & ARITHMETIC CIRCUITS

BOOLEAN ALGEBRA

Understanding Boolean algebra and its laws help us to simplify the Boolean expression so that they contain lesser number of literals. The simplified equation allows us to use lesser number of gates. Therefore the digital circuit we design will be more efficient and also cheaper. We also introduce De Morgan's theorems and using it, we show that NAND/NOR are ***universal gates.*** This chapter is presented under the following headings.

5.1 Laws of Boolean Algebra
5.2 DeMorgan's Theorems
5.3 NAND as Universal gate
5.4 NAND-NAND network
5.5 NOR as Universal gate
5.6 NOR-NOR network
5.7 NOR to OR gate network
5.8 NAND to AND gate network

5.1 LAWS OF BOOLEAN ALGEBRA

Boolean algebra uses only two bits, 0 and 1 and has only two operators + (OR) and . (AND). A number of rules in Boolean algebra are similar to ordinary algebra but a number of other rules are different. Here, we will introduce some of the important Boolean laws and show how they are used to simplify Boolean expressions.

Commutative Law:

The commutative law for addition of two variables is written as

$$A + B = B + A \qquad (5.1)$$

This means that the order in which the variables are OR-ed makes no difference.

Fig. (5.1) illustrates the commutative law applicable to OR gate.

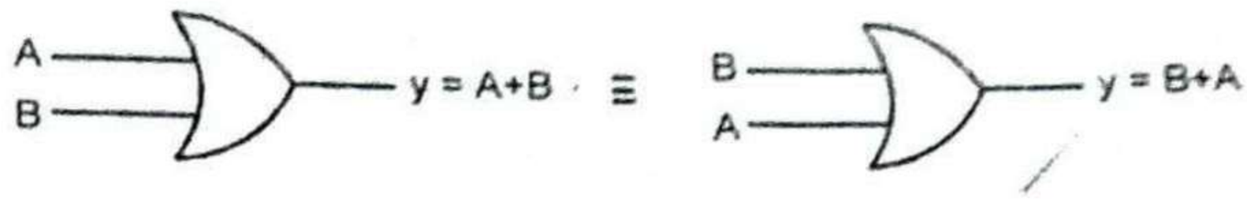

Fig. 5.1

In a similar way, the commutative law for multiplication of two variables is

$$\mathbf{AB = BA} \qquad (5.2)$$

Fig. (5.2) illustrates the commutative law applicable to AND gate.

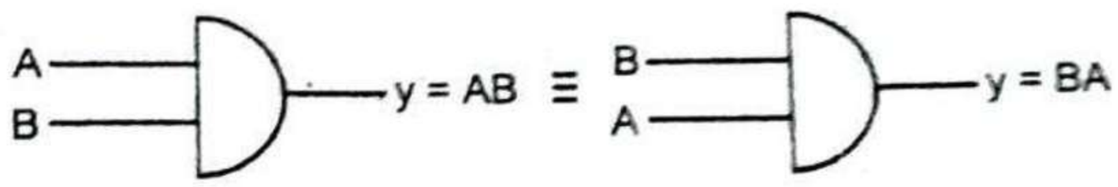

Fig. 5.2

Associative Law:

The associative law for addition of three variables is written as

$$\mathbf{A + (B + C) = (A + B) + C} \qquad (5.3)$$

This means that the result is the same regardless of the order in which the variables are grouped.

Fig. (5.3) illustrates the associative law applicable to OR gate.

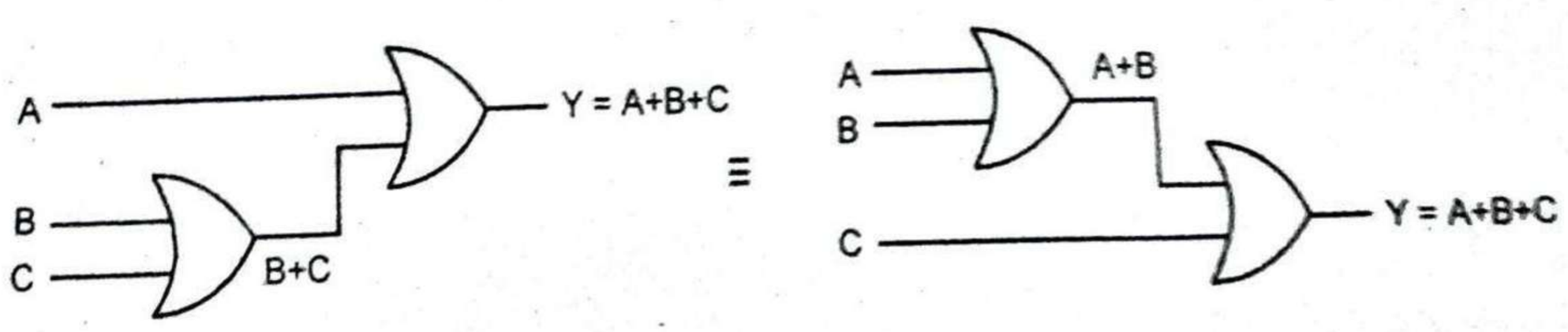

Fig. 5.3

In a similar way, the associative law for multiplication of three variables is

$$A(BC) = (AB)C \qquad (5.4)$$

Fig. (5.4) illustrates the commutative law applicable to AND gate.

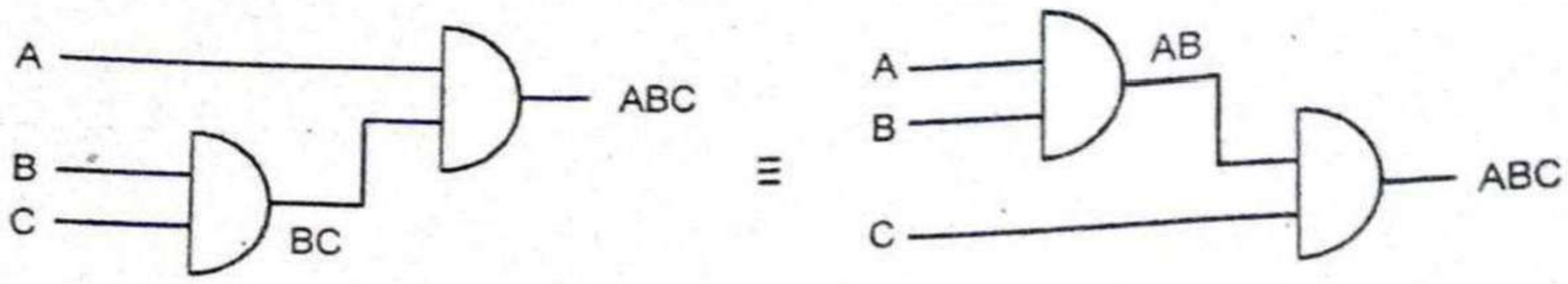

Fig. 5.4

Distributive Law:

The distributive law for three variables is written as

$$A(B + C) = AB + AC \qquad (5.5)$$

Fig. (5.5) illustrates the distributive law.

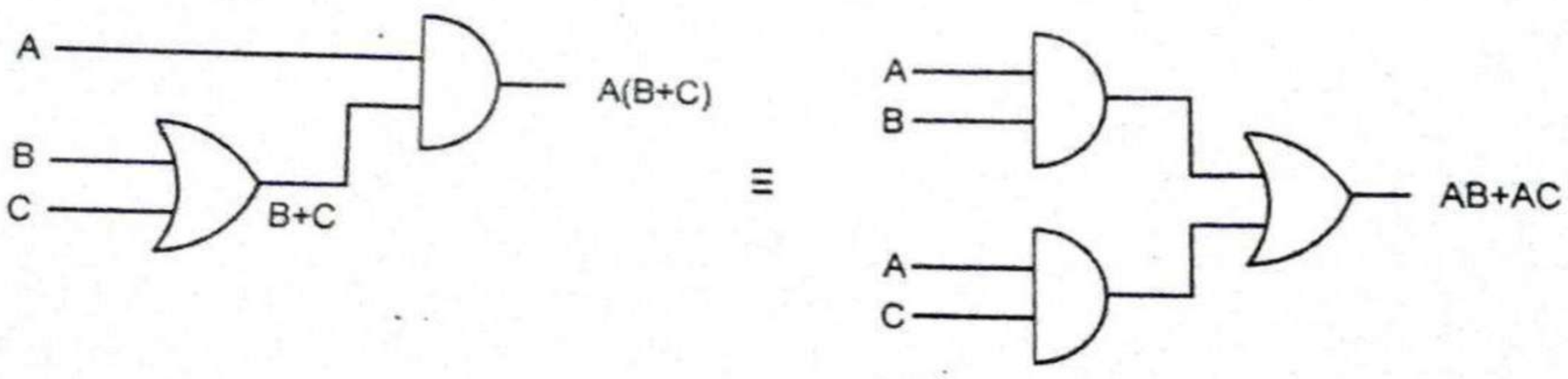

Fig. 5.5

Using a truth table for three variables, the distributive law can be verified.

The commutative law, associative law and distributive law are the same as in ordinary algebra.

Besides the three basic laws discussed above, there are some more standard rules that are specific to Boolean algebra. In order to identify the rules, let us give them numbers. In most cases, the proof is elementary in nature.

Rule 1a: A + 0 = A

When A = 0,

A + 0 = 0 + 0 = 0 = A

When A = 1,

A + 0 = 1 + 0 = 1 = A

Therefore,

A + 0 = A

This rule is illustrated in Fig. 5.6

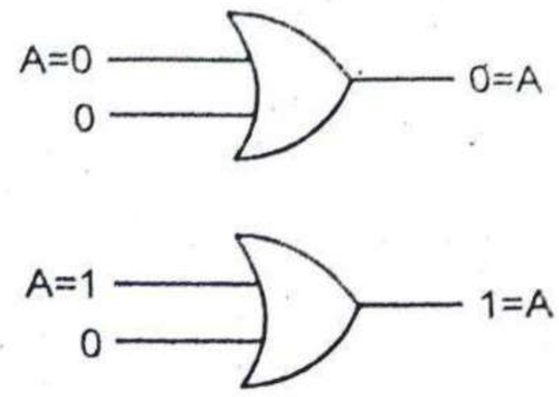

Fig. 5.6

Rule 1b: A.1 = A

When A = 0,

A .1 = 0 .1 = 0 = A

When A = 1,

A .1 = 1 . 1 = 1 = A

Therefore,

A .1 = A

This rule is illustrated in Fig. 5.7

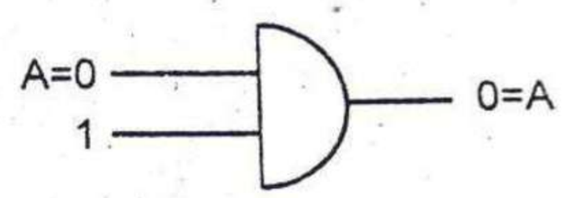

Fig. 5.7

Rule 2a: A + 1 = 1

When A = 0,

A + 1 = 0 + 1 = 1

When A = 1,

A + 1 = 1 + 1 = 1

Therefore,

A + 1 = 1

This rule is illustrated in Fig. 5.8

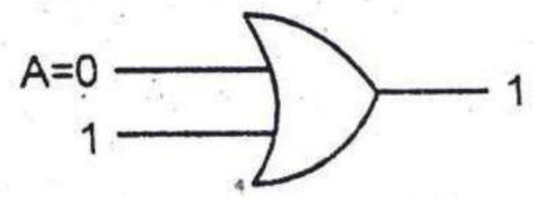

Fig. 5.8

Rule 2b: **A.0 = 0**

When A = 0,

A .0 = 0 .0 = 0

When A = 1,

A .0 = 1 . 0 = 0

Therefore,

A .0 = 0

This rule is illustrated in Fig. 5.9

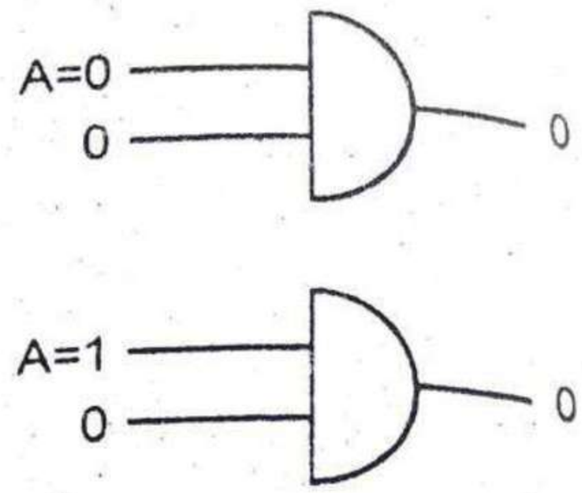

Fig. 5.9

Rule 3a: **A + A = A**

When A = 0,

A + A = 0 + 0 = 0 = A

When A = 1,

A + A = 1 + 1 = 1 = A

Therefore,

A + A = A

This rule is illustrated in Fig. 5.10

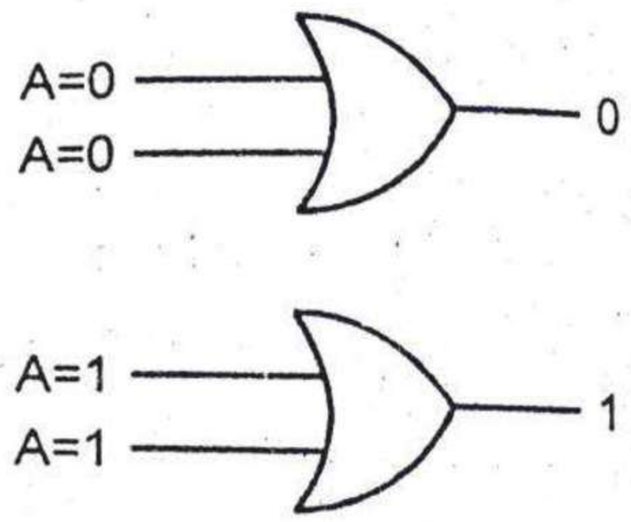

Fig. 5.10

Rule 3b: **A.A = A**

When A = 0,

A .A = 0 .0 = 0 = A

When A = 1,

A .A = 1 . 1 = 1 = A

Therefore,

A.A = A

This rule is illustrated in Fig. 5.11

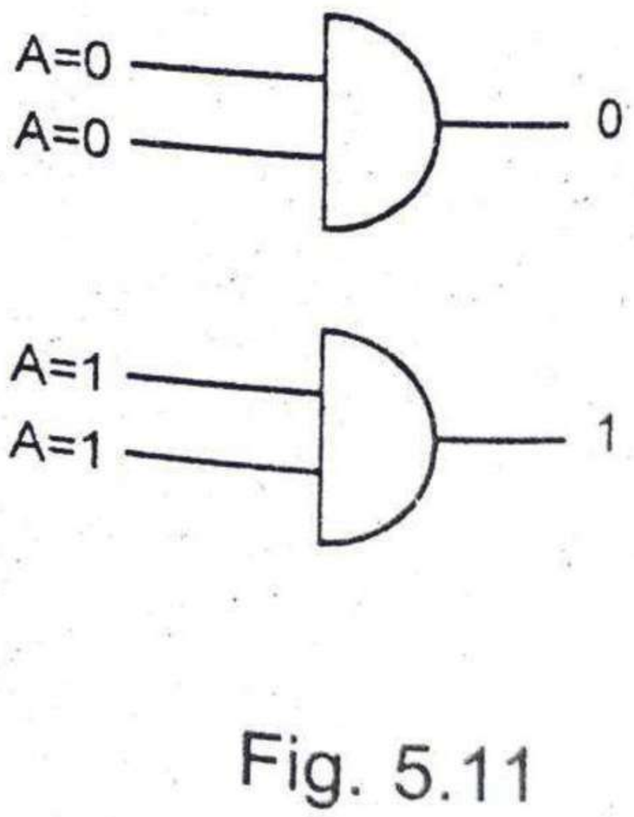

Fig. 5.11

Rule 4a: $A + \overline{A} = 1$

When A = 0,

$A + \overline{A} = 0 + 1 = 1$

When A = 1,

$A + \overline{A} = 1 + 0 = 1$

Therefore,

$A + \overline{A} = 1$

This rule is illustrated in Fig. 5.12

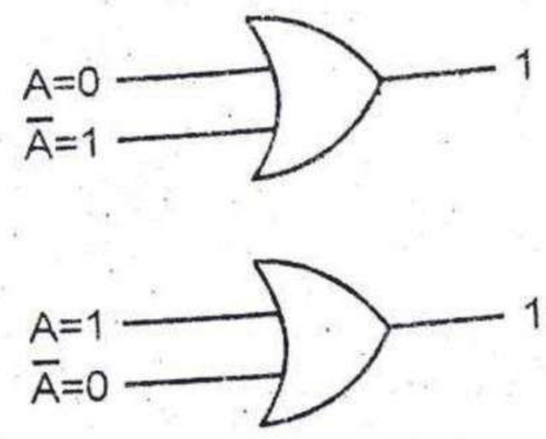

Fig. 5.12

Rule 4b: $A.\overline{A} = 0$

When A = 0,

$A.\overline{A} = 0.1 = 0$

When A = 1,

$A.\overline{A} = 1.0 = 0$

Therefore,

$A.\overline{A} = 0$

This rule is illustrated in Fig. 5.13

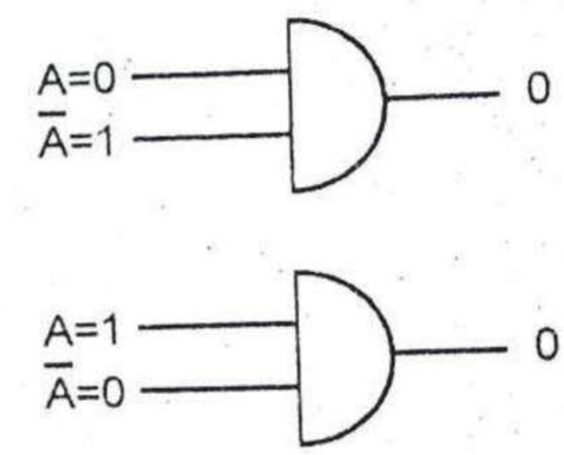

Fig. 5.13

Rule 5: $\overline{\overline{A}} = A$

When A = 0,

$\overline{A} = 1$; $\overline{\overline{A}} = 0 = A$

When A = 1,

$\overline{A} = 0$; $\overline{\overline{A}} = 1 = A$

Therefore,

$\overline{\overline{A}} = A$

This rule is illustrated in Fig. 5.14

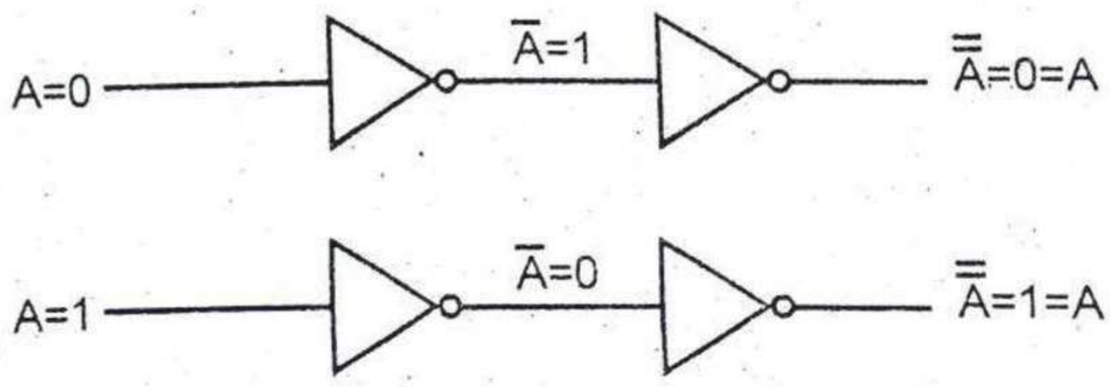

Fig. 5.14

This double complement rule is also called as ***involution***.

Rule 6a: **A + AB = A**

Method 1:

L.H.S = A + AB

= A(1+B)

= A.1 ; for 1 + B = 1

= A ; for A.1 = A

A + AB = A

This rule can be proved using the above rules or by truth table.

Method 2: Using truth table:

A	B	AB	A + AB
0	0	0	0
0	1	0	0
1	0	0	1
1	1	1	1

Comparing columns 1 and 4, it follows that

A + AB = A

This method of using the truth table to prove an identity is called '***proof by perfect induction***'

Rule 6b: **A (A+ B) = A**

Method 1:

L.H.S = A(A + B)

= AA + AB

= A + AB ; for AA = A

= A ; Rule 6a

= RHS

Therefore,

A (A+ B) = A

Method 2: Using truth table:

A	B	A + B	A(A + B)
0	0	0	0
0	1	1	0
1	0	1	1
1	1	1	1

Comparing columns 1 and 4, it follows that

$$A(A+ B) = A$$

Rules 6a and 6b are also called as laws of **absorption.**

Rule 7a: $\mathbf{A + \bar{A}B = A + B}$

Proof 1:

$$\begin{aligned} \text{LHS} &= A + \bar{A}B \\ &= A.1 + \bar{A}B && \text{; for } A.1 = A \\ &= A(1 + B) + \bar{A}B && \text{; for } 1 + B = 1 \\ &= A + AB + \bar{A}B \\ &= A + B(A + \bar{A}) \\ &= A + B && \text{; for } A + \bar{A} = 1 \\ &= \text{RHS} \end{aligned}$$

Therefore,

$$A + \bar{A}B = A + B$$

Proof 2:

$$\begin{aligned} \text{RHS} &= A + B \\ &= A + B.1 \\ &= A + B(A + \bar{A}) && \text{; for } A + \bar{A} = 1 \\ &= A + BA + B\bar{A} \\ &= A + AB + \bar{A}B && \text{; for } AB = BA \\ &= A + \bar{A}B && \text{; for } A + AB = A \\ &= \text{LHS} \end{aligned}$$

Therefore,

$$A + \overline{A}B = A + B$$

The identity can also be proved simply, using a truth table. But of course, using basic rules to prove some other rules is more elegant.

Rule 7b: $\mathbf{A(\overline{A} + B) = A.B}$

Proof:

$$\begin{aligned} \text{LHS} &= A(\overline{A} + B) \\ &= A\overline{A} + AB \\ &= AB \qquad ; \text{for } A\overline{A} = 0 \\ &= \text{RHS} \end{aligned}$$

Therefore,

$$A(\overline{A} + B) = AB$$

Rule 8a: $\mathbf{A + BC = (A + B)(A + C)}$

Proof:

$$\begin{aligned} \text{RHS} &= (A + B)(A + C) \\ &= AA + AB + AC + BC \\ &= A + AB + AC + BC \qquad ; \text{for } AA = A \\ &= A(1 + B + C) + BC \\ &= A + BC \qquad ; \text{for } 1 + B + C = 1 \end{aligned}$$

Hence $A + BC = (A + B)(A + C)$

Note:

Since $A + BC = (A + B)(A + C)$ it follows

$A + \overline{B}C = (A + \overline{B})(A + C)$

$\overline{A} + \overline{B}\overline{C} = (\overline{A} + \overline{B})(\overline{A} + \overline{C})$

Rule 8b: $\mathbf{A(B + C) = AB + AC}$

This is only a distributive law.

Rule 9a: $\mathbf{AB + \bar{A}C + BC = AB + \bar{A}C}$

Proof:

Comparing LHS and RHS, we can see that the term BC on the LHS is the term to be removed to make both sides equal.

$$
\begin{aligned}
\text{LHS} &= AB + \bar{A}C + BC \\
&= AB + \bar{A}C + BC.1 \\
&= AB + \bar{A}C + BC(A + \bar{A}) && ;\ A + \bar{A} = 1 \\
&= AB + \bar{A}C + ABC + \bar{A}BC \\
&= AB\,(1 + C) + \bar{A}C\,(1 + B) \\
&= AB + \bar{A}C && ;\ \text{for } 1 + C = 1;\ 1 + B = 1
\end{aligned}
$$

Therefore,

$$AB + \bar{A}C + BC = AB + \bar{A}C$$

A number of similar equations can be formed as given below.

$A\bar{B} + \bar{A}C + \bar{B}C$	=	$A\bar{B} + \bar{A}C$
$\bar{A}B + AC + BC$	=	$\bar{A}B + AC$
$\bar{A}\bar{B} + A\bar{C} + \bar{B}\bar{C}$	=	$\bar{A}\bar{B} + A\bar{C}$
$XY + \bar{X}Z + YZ$	=	$XY + \bar{X}Z$

Rule 9b: $\mathbf{(A + B)(\bar{A} + C)(B + C) = (A + B)(\bar{A} + C)}$

Proof:

$$
\begin{aligned}
\text{LHS} &= (A + B)(\bar{A} + C)(B + C) \\
&= (A\bar{A} + \bar{A}B + AC + BC)(B + C) \\
&= (\bar{A}B + AC + BC)(B + C) && ;\ \text{for } AA = 0 \\
&= \bar{A}BB + ABC + BBC + \bar{A}BC + ACC + BCC \\
&= \bar{A}B + ABC + BC + \bar{A}BC + AC + BC && ;\ \text{for } AA = A,\ BB = B \\
&= \bar{A}B + \bar{A}BC + ABC + BC + AC + BC \\
&= \bar{A}B(1 + C) + BC(A + 1) + AC + BC \\
&= \bar{A}B + BC + AC + BC && ;\ \text{for } 1+C = 1,\ 1 + A = 1 \\
&= \bar{A}B + AC + BC && ;\ \text{for } BC + BC = BC
\end{aligned}
$$

RHS = $(A + B)(\overline{A} + C)$

= $A\overline{A} + \overline{A}B + AC + BC$

= $\overline{A}B + AC + BC$; for $A\overline{A} = 0$

LHS = RHS

Therefore,

$(A + B)(\overline{A} + C)(B + C) = (A + B)(\overline{A} + C)$

DUALITY PRINCIPLE

We have seen that Rule 1 to Rule 7 (except for Rule 5) are given in pairs. They are taken as 1a and 1b, 2a and 2b etc. If Rule 1a is given, 1b can be obtained; if Rule 2a is given, 2b can be obtained etc.. In all these cases, if one rule is given, the other one of the pair can be obtained by interchanging the binary operators OR and AND and by replacing1's with 0's and 0's with 1's. This property is called **duality principle.** For example, A + 0 = A is a dual of A.1 = A. Similarly A + 1 = 1 is the dual of A.0 = 0.

Given a Boolean rule, the dual can be obtained by,

i) changing each OR sign to AND sign

ii) changing each AND sign to OR sign

iii) complementing any 0 or 1 present in the expression.

We give below some Boolean rules and their duals.

1a: A + 0 = A	**1b: A.1 = A**
2a: A + 1 = 1	**2b: A.0 = 0**
3a: A + A = A	**3b: A.A = A**
4a: $A + \overline{A} = 1$	**4b: $A.\overline{A} = 0$**
5a: $\overline{\overline{A}} = A$	**5b: $\overline{\overline{A}} = A$**
6a: A + AB = A	**6b: A (A+ B) = A**
7a: $A + \overline{A}B = A + B$	**7b: $A(\overline{A} + B) = A.B$**
8a: A + BC = (A + B) (A + C)	**8b: A(B + C) = AB + AC**
9a: $AB + \overline{A}C + BC = AB + \overline{A}C$	**9b: $(A + B)(\overline{A} + C)(B + C) = (A + B)(\overline{A} + C)$**

With the help of the laws and rules we have discussed so far, it is possible to simplify a given Boolean expression. Without proof (since it is straightforward), we can write some more identities.

For example, we have,

$$A + 1 = 1 \qquad \text{; Rule 2a}$$

It follows that,

$$A + B + 1 = 1$$
$$A + AB + 1 = 1$$
$$AB + ABC + A\bar{B}CD + 1 = 1$$
$$A + ABC + \text{- - - - - - - - - - -} + 1 = 1$$

This means that, in a Sum of Product expression, if one of the terms is 1, then the output is 1.

We have,

$$A + A = A \qquad \text{;Rule 3a}$$
$$A + AB = A \qquad \text{;Rule 6a}$$

It can be shown easily that,

$$A + A + A = A$$
$$A + AB + ABC = A$$
$$A + ABD + ADEF + ACEFG = A$$

Let us take Rule 7a,

$$A + \bar{A}B = A + B$$

We can write a number of similar rules.

$$A + \bar{A}\bar{B} = A + \bar{B}$$
$$\bar{A} + AB = \bar{A} + B$$
$$\bar{A} + A\bar{B} = \bar{A} + \bar{B}$$
$$A + \bar{A}BC = A + BC$$
$$X + \bar{X}YZ = X + YZ$$

All the above expressions can be easily proved as we have done for Rule 7a.

Let us try some examples, which make use of the Boolean rules.

5.2 De MORGAN'S THEOREMS

De Morgan has introduced two theorems. We will take them one by one, give the statement and prove by perfect induction.

Theorem 1:

$$\overline{AB} = \bar{A} + \bar{B}$$

"The complement of a product is equal to the sum of (individual) complements."

The proof is given using truth table.

A	B	$\bar{A}$	$\bar{B}$	AB	$\overline{AB}$	$\bar{A}+\bar{B}$
0	0	1	1	0	1	1
0	1	1	0	0	1	1
1	0	0	1	0	1	1
1	1	0	0	1	0	0

The last two columns are equal and hence $\overline{AB} = \bar{A} + \bar{B}$

Note:

The expression on the LHS, $\overline{AB}$ corresponds to a NAND gate. The equation on the RHS can be implemented using two NOT gates and one OR gate. This is shown in Fig. 5.17a.

Fig. 5.17a

The circuit in Fig.5.17a can also be modified as shown in Fig. 5.17b.

Fig. 5.17b

Here the NOT gates in front of the OR gate have been removed and in their place just bubbles are drawn, the bubble indicating inversion. This arrangement is called bubbled OR gate. Therefore, we can write,

NAND = Bubbled OR

Theorem 2:

$$\overline{A+B} = \overline{A} \cdot \overline{B}$$

"The complement of a sum is equal to the product of (individual) complements."

The proof is given using truth table.

A	B	$\overline{A}$	$\overline{B}$	A+B	$\overline{A+B}$	$\overline{A}.\overline{B}$
0	0	1	1	0	1	1
0	1	1	0	1	0	0
1	0	0	1	1	0	0
1	1	0	0	1	0	0

Fig. 5.18

The last two columns are equal and hence $\overline{A+B} = \overline{A}.\overline{B}$

Note:

The expression on the LHS, $\overline{A+B}$ corresponds to a NOR gate. The equation on the RHS can be implemented using two NOT gates and one AND gate. This is shown in Fig. 5.18a.

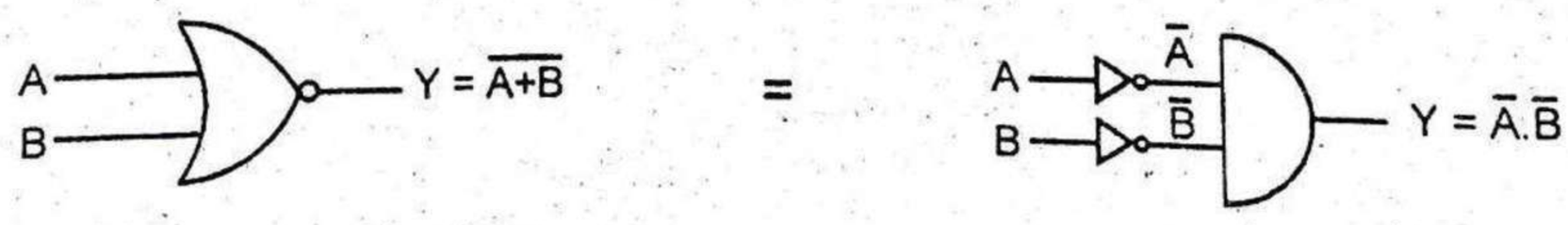

Fig. 5.18a

The circuit in Fig.5.18a can also be modified as shown in Fig. 5.18b.

Fig. 5.18b

Here, the NOT gates in front of the AND gate have been removed and in their place just bubbles are drawn, the bubble indicating inversion. This arrangement is called bubbled AND gate. Therefore, we can write,

NOR = Bubbled AND

DeMorgan's theorems are applicable to more than two variables also. Let us take some examples.

From the first DeMorgan's theorem,

$$\overline{AB} = \overline{A} + \overline{B}$$

It follows,

$$\overline{ABC} = \overline{A} + \overline{B} + \overline{C}$$
$$\overline{ABCD} = \overline{A} + \overline{B} + \overline{C} + \overline{D}$$
$$\overline{ABC.....Z} = \overline{A} + \overline{B} + \overline{C} + ... + \overline{Z}$$

From the second DeMorgan's theorem,

$$\overline{A+B} = \overline{A}.\overline{B}$$

It follows,

$$\overline{A+B+C} = (\overline{A} + \overline{B})\,\overline{(C + D)}$$
$$\overline{A+B+C+D} = \overline{A}.\,\overline{B}.\overline{C}.\,\overline{D}$$
$$\overline{A+B+C+.....Z} = \overline{A}.\overline{B}.\overline{C}. .... \overline{Z}$$

Example 5.12

Use DeMorgan's theorem to find the complement of A + BC.

Solution:

$$\overline{A + BC} = \overline{A} \,.\, \overline{BC}$$
$$= \overline{A}\,(\overline{B} + \overline{C})$$

Example 5.13

Find the complement of $A\overline{B} + \overline{C}\,\overline{D}$ and simplify.

Solution:

$$\overline{A\overline{B} + \overline{C}\,\overline{D}} = \overline{A\overline{B}} \,.\, \overline{\overline{C}\,\overline{D}}$$
$$= (\overline{A} + \overline{\overline{B}})\,(\overline{\overline{C}} + \overline{\overline{D}}) = (\overline{A} + B)\,(C + D)$$

Example 5.14

Find the complement of $(A + B)(B + C)(C + A)$.

Solution:

$$\overline{(A + B)(B + C)(C + A)} = \overline{(A + B)} + \overline{(B + C)} + \overline{(C + A)}$$
$$= \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{C}\bar{A}$$

Example 5.15

Find the complement of $A + \overline{B + \overline{CD}}$.

Solution:

$$\overline{A + \overline{B + \overline{CD}}} = \bar{A} \cdot \overline{\overline{B + \overline{CD}}}$$
$$= \bar{A}\,(B + \overline{CD})$$
$$= \bar{A}\,(B + \bar{C} + \bar{D})$$

Example 5.16

Show that $\overline{\bar{A}B + A\bar{B}} = \bar{A}\bar{B} + AB$.

Solution:

$$\overline{\bar{A}B + A\bar{B}} = \overline{\bar{A}B} \cdot \overline{A\bar{B}}$$
$$= (\bar{\bar{A}} + \bar{B})(\bar{A} + \bar{\bar{B}})$$
$$= (A + \bar{B})(\bar{A} + B)$$
$$= A\bar{A} + \bar{A}\bar{B} + AB + B\bar{B}$$
$$= \bar{A}\bar{B} + AB \qquad \text{; for } A\bar{A} = 0,\ B\bar{B} = 0.$$

That is, complementing the XOR expression gives the XNOR expression.

Example 5.17

Show that $\overline{\bar{A}\bar{B} + AB} = \bar{A}B + A\bar{B}$.

Solution:

$$\overline{\bar{A}\bar{B} + AB} = \overline{\bar{A}\bar{B}} \cdot \overline{AB}$$
$$= (\bar{\bar{A}} + \bar{\bar{B}})(\bar{A} + \bar{B})$$
$$= (A + B)(\bar{A} + \bar{B})$$
$$= A\bar{A} + \bar{A}B + A\bar{B} + B\bar{B}$$
$$= \bar{A}B + A\bar{B}$$

: for $A\bar{A} = 0,\ B\bar{B} = 0.$

That is, complementing the XNOR expression gives the XOR expression.

ARITHMETIC CIRCUITS

In this chapter, arithmetic circuits are introduced. By combining logic circuits in the right way, we can build circuits that add and subtract binary numbers. We will introduce adder and subtractor circuits. We will also discuss how only adder circuits are used to perform addition as well as subtraction. This chapter covers the following headings.

8.1 Binary addition

8.2 Half adder and Full adder

8.3 Four bit binary adder

8.4 BCD adder

8.5 Half subtractor and Full subtractor

8.6 Four bit adder/subtractor circuit

8.1 BINARY ADDITION

We have already discussed in detail binary arithmetic operations in Chapter 2 (Binary Arithmetic). Let us recollect the rules for binary addition.

Four basic cases of binary addition are

$$0 + 0 = 0$$

$$0 + 1 = 1$$

$$1 + 0 = 1$$

$$1 + 1 = 10$$

The last rule namely 1 + 1 = 10 means that 1 + 1 is equal to 2 and 2 in binary is 10. We will read this as 0 carry 1. Using this rule, let us perform one simple addition. We have already seen some examples in Chapter 2, Sec 2.1.

Example 8.1

Add 12 and 13 in binary.

Solution:

Carry:	1 1	
12 +	1 1 0 0 +	
13	1 1 0 1	
25	1 1 0 0 1	

We see that the carry produced out of an addition in one column is taken to the next higher column and added (similar to decimal addition).

8.2 HALF ADDER and FULL ADDER:

Half Adder:

Half adder is a logic circuit that adds two bits and gives the result on two output lines as sum (S) and carry (Cy).

Let A and B be two inputs and S and Cy the two outputs. The block diagram for a half adder is shown in Fig. 8.1.

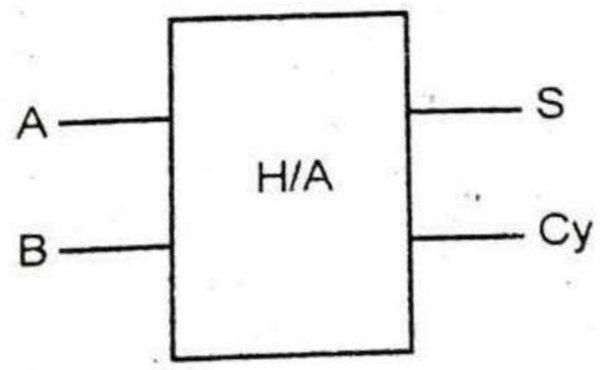

Fig. 8.1

Since A and B can take values 0 or 1, the total number of possible input combinations is four. The inputs and the corresponding outputs can be represented in a truth table as shown in Fig. 8.2.

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Fig. 8.2

From the truth table, the sum of product expressions for sum and carry can be written as

$$\text{Sum} = \bar{A}B + A\bar{B}$$

and $$\text{Carry} = AB$$

These two expressions can be implemented using the circuit shown in Fig. 8.3.

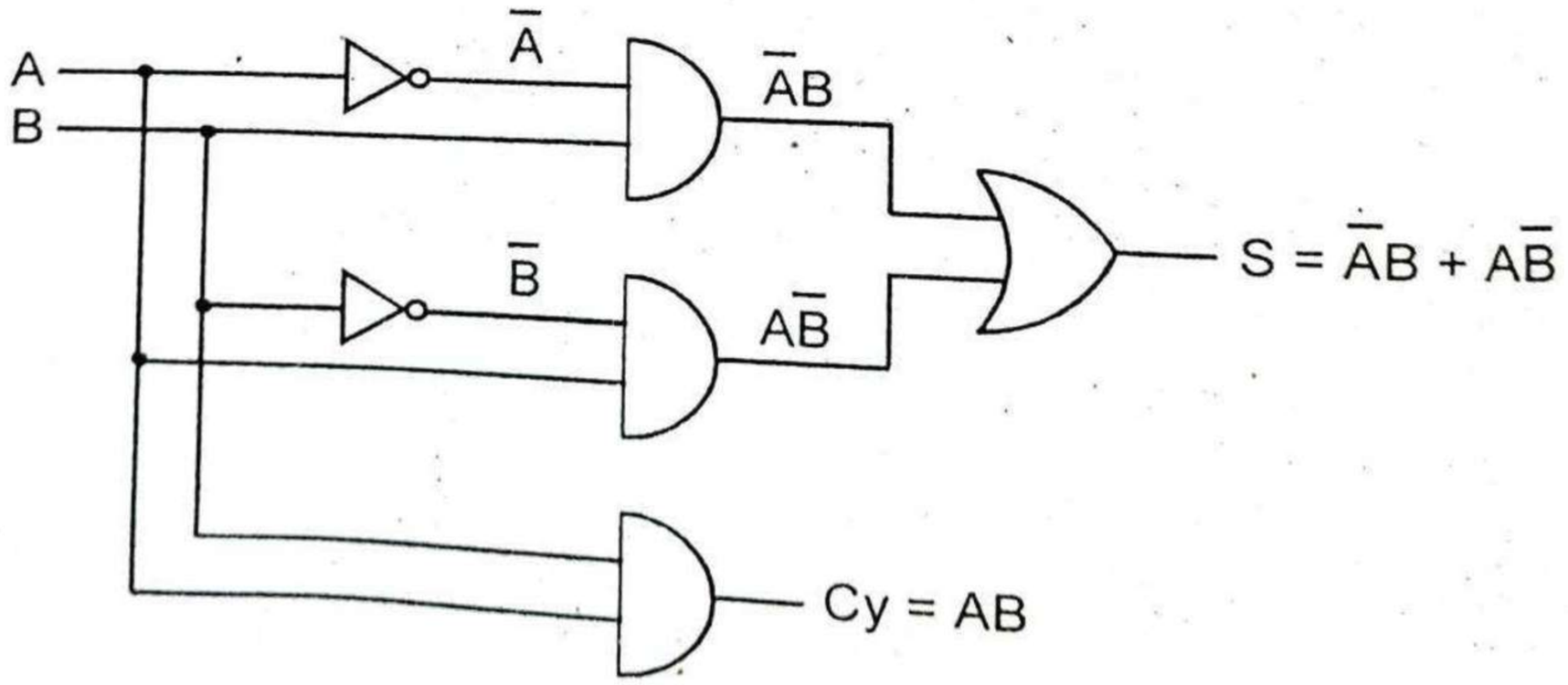

Fig. 8.3

But since the Sum expression is directly an Ex-OR expression, the half adder circuit can also be drawn as Fig. 8.4.

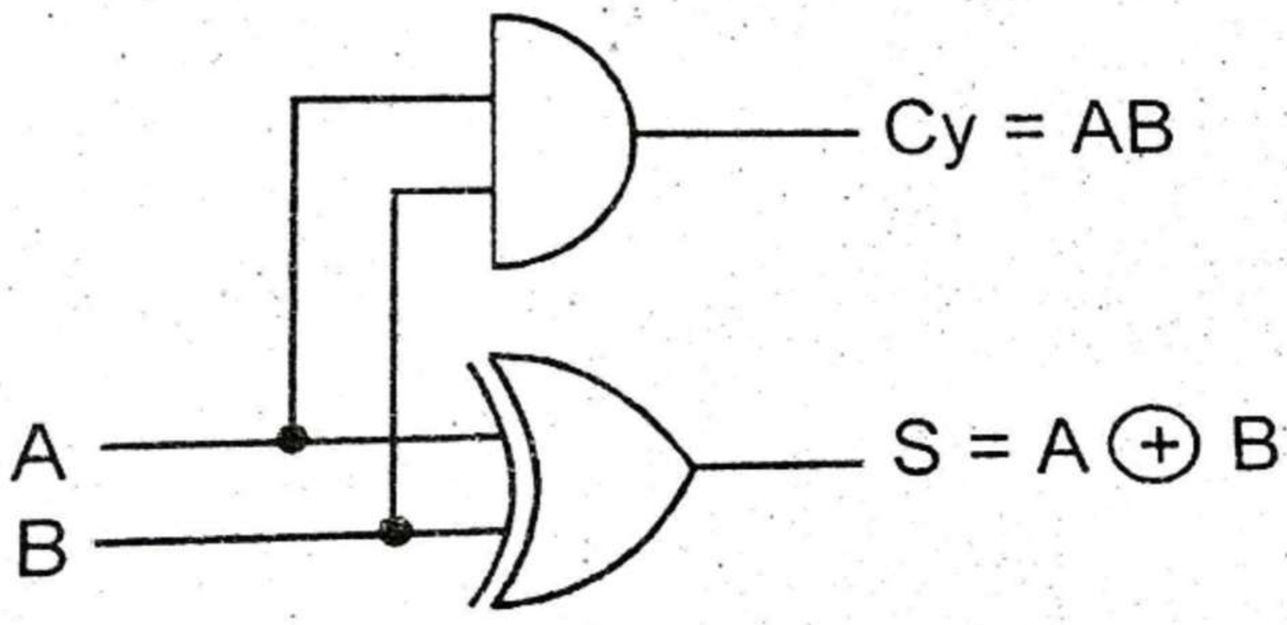

Fig. 8.4

Full Adder:

A full adder is a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs. Two of the input variables denoted by A and B

represent the two significant bits to be added. The third input C represents the carry from the previous lower significant position. The two outputs are designated as S for sum and Cy for carry. The block diagram of a full adder is shown in Fig. 8.6.

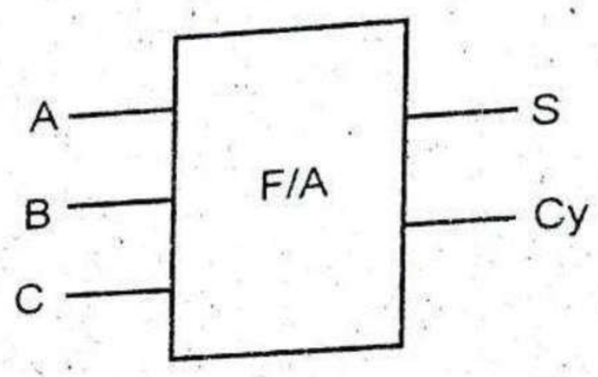

Fig. 8.6

The truth table of the full adder is given in Fig. 8.7.

A	B	C	S	Cy
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Fig. 8.7

Note that with three inputs, we have eight (2^3) combinations.

Both sum and carry can be represented in Boolean expressions in sum of products form. They can be simplified and a logic circuit can be implemented for the full adder.

We can implement a full adder using the above expressions. The required circuit is given in Fig. 8.11.

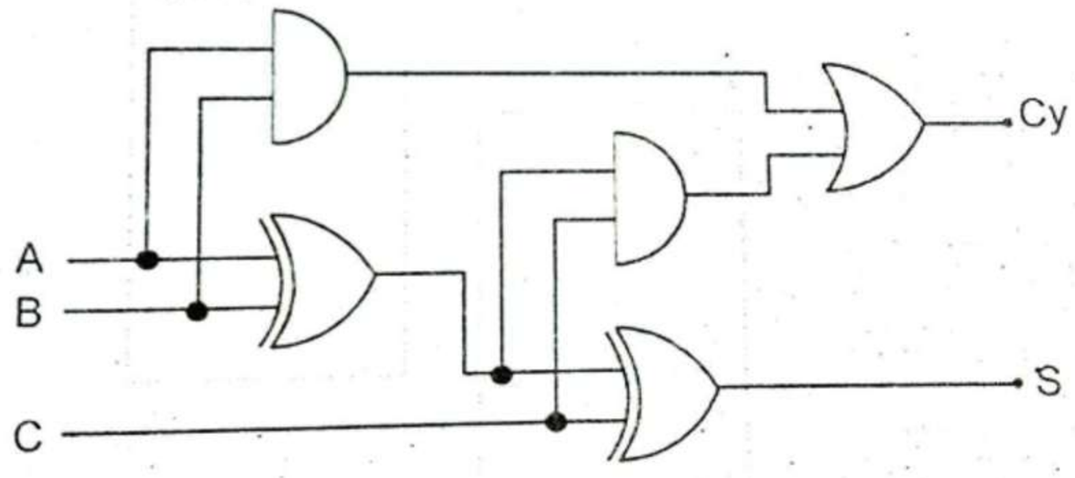

Fig. 8.11

The full adder circuit shown in Fig 8.11 can be seen to be made up of two half adders and an OR gate. The block diagram representation is given in Fig. 8.12.

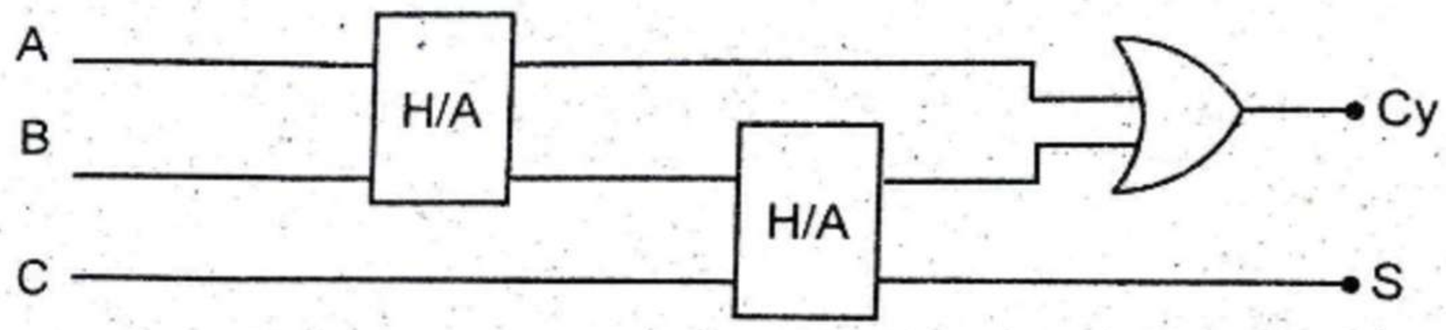

Fig. 8.12

The sum output of the first half adder is added with the third input using a second half adder. The carry outputs of the first and second half adders are combined using an OR gate to produce a single final carry.

With reference to Fig 8.18, we can see that the sum output $Y_3Y_2Y_1Y_0$ is directly connected to the augend inputs of the second 4-bit adder. The LSB and MSB of the addend inputs of the second 4-bit adder are kept in '0' state. The remaining two inputs are connected together and connected to the X output of the circuit discussed. With this arrangement the correction factor of six is added only when required. For the second 4-bit adder also the Cy_{in} input is kept in '0' state. The Cy_{out} of the first 4-bit adder itself gives the final carry when BCD result exceeds nine.

The AND-OR circuit, to add six can be replaced by a NAND-NAND circuit (carry output of the first 4-bit adder also need to be inverted).

8.5 HALF SUBTRACTOR AND FULL SUBTRACTOR:

Half Subtractor:

Half subtractor is a logic circuit that subtracts one bit from another bit and produces two outputs as Difference (Diff) and Borrow (Br). The rules for binary subtraction are given below (Refer Chapter 2).

$0 - 0 = 0$

$0 - 1 = 1$ with a borrow 1

$1 - 0 = 1$

$1 - 1 = 0$

With A and B as two inputs, and Diff and Br as the two outputs, the block diagram for a half subtractor is as shown in Fig. 8.19.

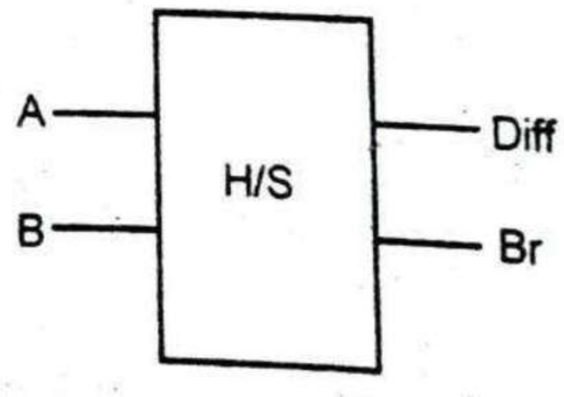

Fig. 8.19

There are four possible input combinations for A and B. The input combinations and the corresponding outputs can be drawn as a truth table shown in Fig. 8.20.

A	B	Diff	Br
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Fig. 8.20

From the truth table, the Boolean expressions for Diff and Br are found to be

$$\text{Diff} = \bar{A}B + A\bar{B}$$

and $$\text{Br} = \bar{A}B$$

These two expressions can be implemented using the circuit shown in Fig. 8.21.

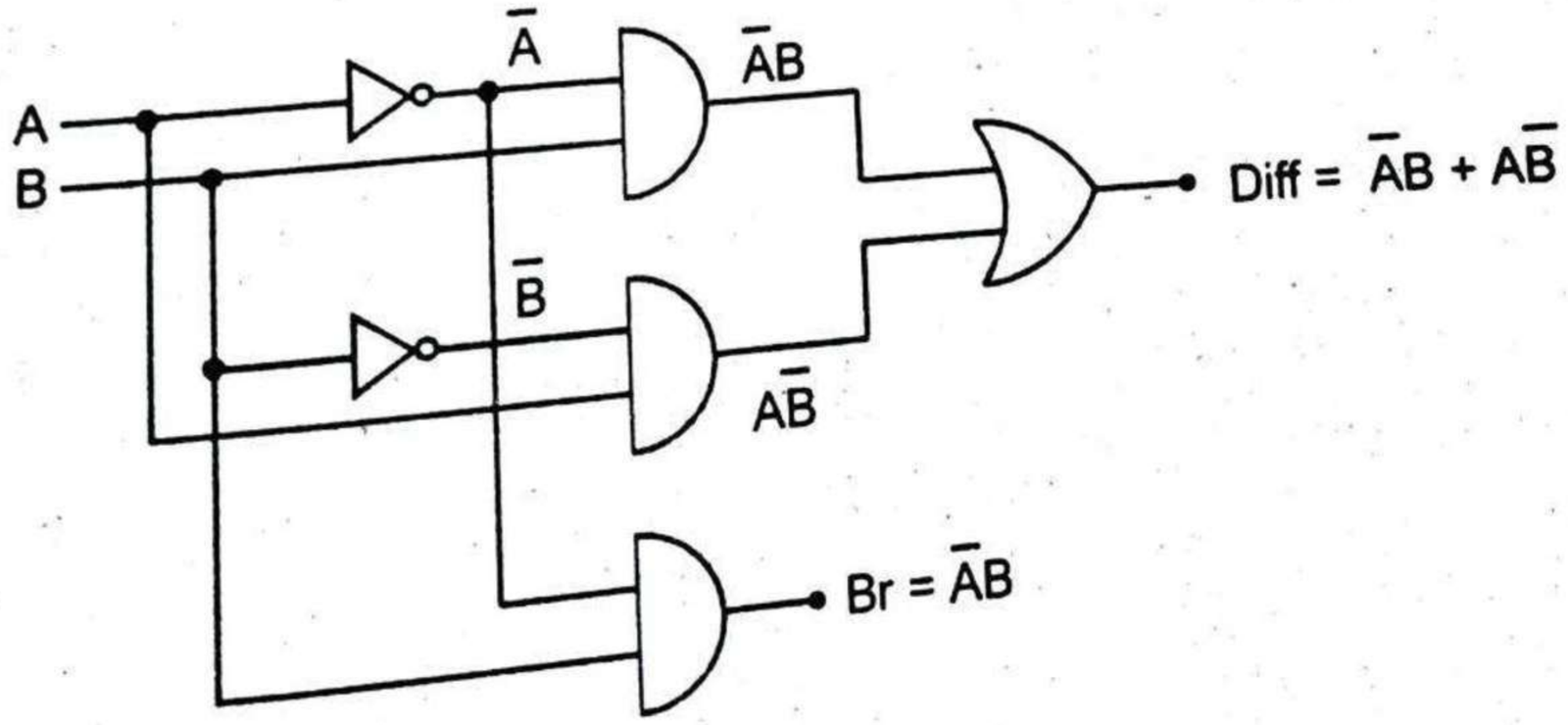

Fig. 8.21

As in the case of half adder, here also we can see that the difference output can be taken directly from an Ex-OR gate.

The required circuit is given in Fig. 8.22.

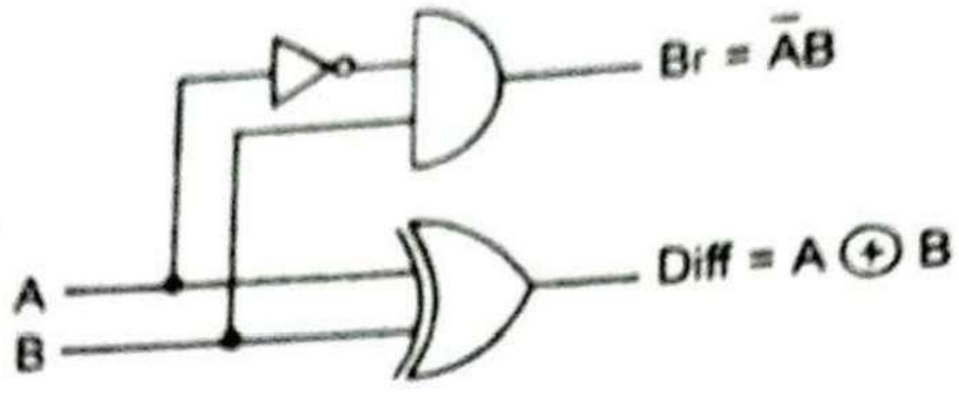

Fig. 8.22

Half Subtractor using NAND gates:

We have already seen how to get an Ex-OR using NAND gates. The output of the Ex-OR arrangement gives the difference. However to get the borrow, the AND gate is not replaced by two NAND gates. Instead the output of the NAND gate (G_3) (=$\overline{B.\overline{AB}}$) is inverted using another NAND gate (G_5) to get the borrow = $\bar{A}B$. If the AND gate is replaced by NAND gates, we would have required two NAND gates. This way the number of NAND gates required is reduced by one. The half subtractor circuit using only NAND gates is shown in Fig. 8.23.

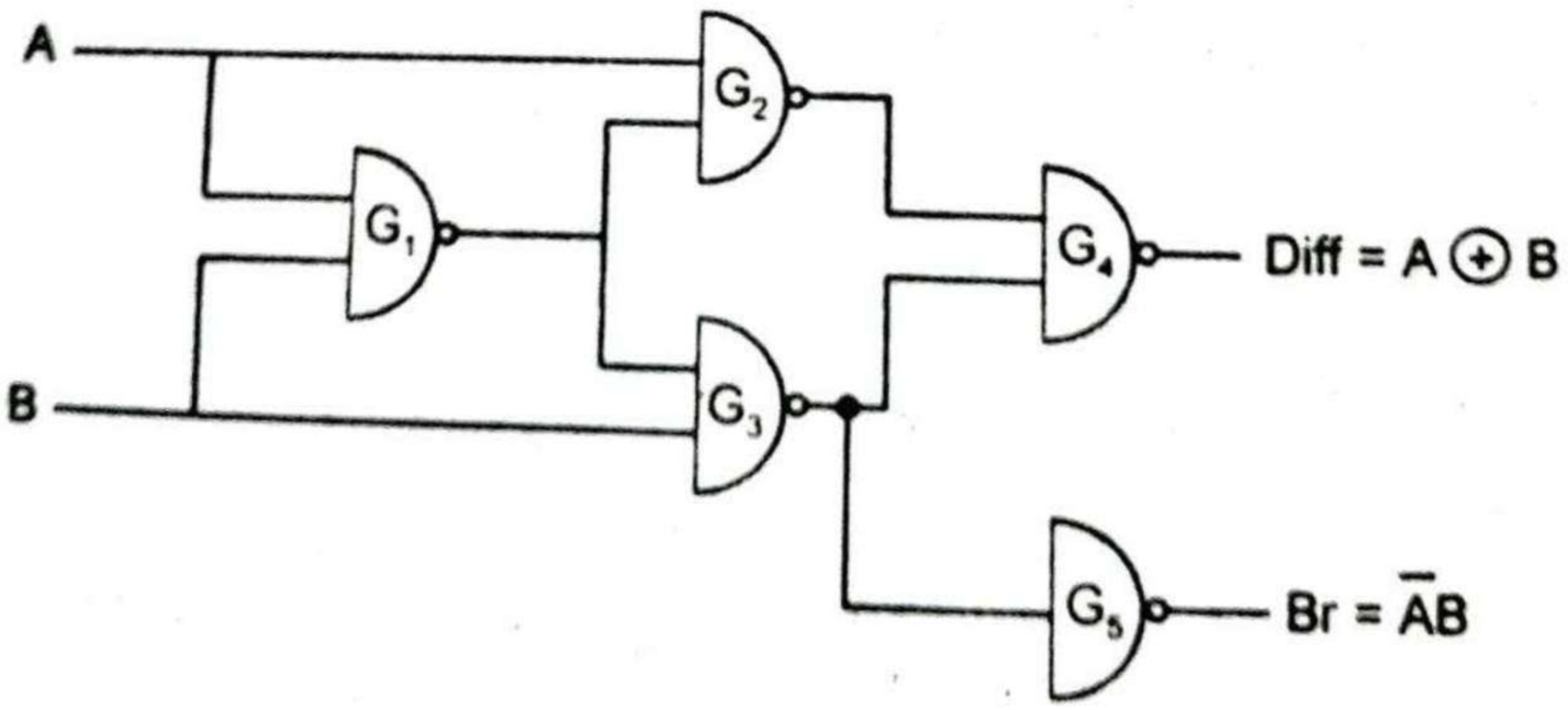

Fig. 8.23

In a similar way, a half subtractor can also be implemented using NOR gates only.

Full Subtractor:

A full subtractor is a combinational circuit that performs the arithmetic subtraction of three input bits. It consists of three inputs and two outputs. Two of the input variables denoted by A and B represent the two significant bits to be subtracted. The third input C represents the borrow taken from the next higher significant position. The two outputs are designated as Diff for difference and Br for borrow. The block diagram of a full subtractor is shown in Fig. 8.24.

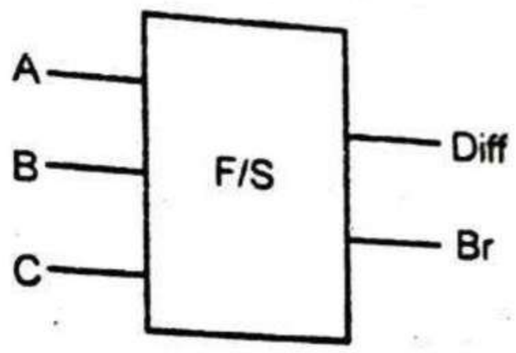

Fig. 8.24

The truth table of the full subtractor is given in Fig. 8.25.

A	B	C	Diff	Br
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Fig. 8.25

Both Diff and Br can be represented in Boolean expressions in sum of products form. They can be simplified and a logic circuit can be implemented for the full subtractor. Here

UNIT-I: CURRENT ELECTRICITY

OHM'S LAW & KIRCHOFF'S LAWS & THE APPLICATIONS

a. Ohm's law:

The current flow through a conductor depends upon the potential difference applied.

Ohm's law states that when the temperature remains constant, the potential difference between the ends of the conductor is directly proportional to the current flowing through the conductor.

Potential difference $\propto$ current

or $V \propto I$ or $\frac{V}{I} = \text{constant } R$

$\therefore V = IR$

Here R is a constant called the resistance of the conductor. It is measured in the unit of ohm. When the p.d is measured in volt and the current in ampere, then,

$$1 \text{ ohm} = \frac{1 \text{ volt}}{1 \text{ ampere}}$$

From this we can define the unit of resistance. **The ohm is defined as the resistance of a conductor in which a potential difference of 1 volt is developed when current of 1 ampere flows through it or simply ohm is the ratio between volt and ampere.**

Verification of ohm's law:

Ohm's law can be verified using a simple circuit shown in fig3.10. The current through the circuit can be varied with the help of a rheostat connected in series with the battery. The current can be measured using the ammeter. The p.d across the resistance R can be measured using the voltmeter V.

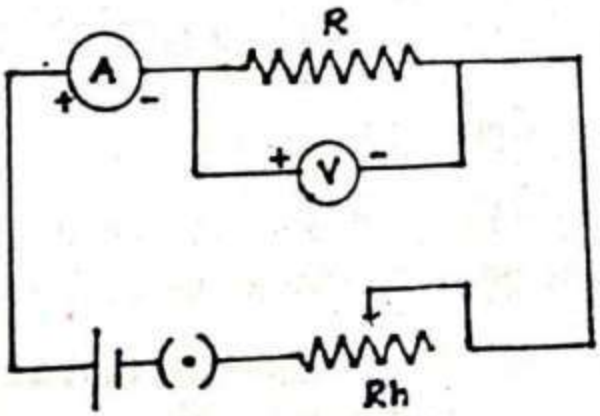

Fig 3.10

Using the rheostat, the current through the circuit is kept at a particular value I. Now the voltmeter reading is noted. Let it be V. Then V/I is calculated. Similarly by changing the current, for each current the p.d across the resistance is noted. For each current V/I is calculated. It is found to be a constant. This verifies the Ohm's law.

b. Kirchhoff's Law

In a simple circuits consisting of battery and resistance in series or parallel, we can apply Ohm's law to calculate the current and the potential differences. If the circuit is complicated we cannot use Ohm's law. For such a circuits Kirchhoff's law can be used.

(i) ***Kirchhoff's First Law:*** **In any network of conductors in an electrical circuit, the algebraic sum of currents meeting at any point is zero or sum of the currents flowing towards a point is equal to the sum of currents flowing away form it.**

$$\Sigma I = 0 \qquad (1)$$

For example let a number of conductors meet at a junction as shown in fig3-11. Let I_1, I_2, I_3, I_4 and I_5 be currents flowing. Generally the currents flowing towards the points are taken as positive whereas the currents flowing away from the points are taken as negative. According to first law,

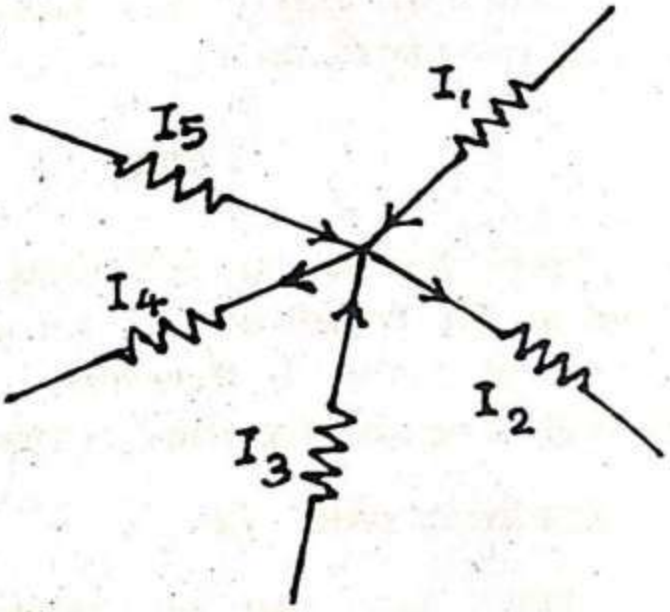

Fig 3.11

$$I_1 - I_2 + I_3 - I_4 + I_5 = 0$$

or $$I_1 + I_3 + I_5 = I_2 + I_4 \qquad (2)$$

The first law is based on the principle that in an electric circuit, at any point the charge cannot be accumulated.

(ii) ***Kirchhoff's Second Law:*** **In a closed path of networks of conductors, the algebraic sum of the products of resistance**

and current of each part of the closed path is equal to the algebraic sum of e.m.fs in the circuit.

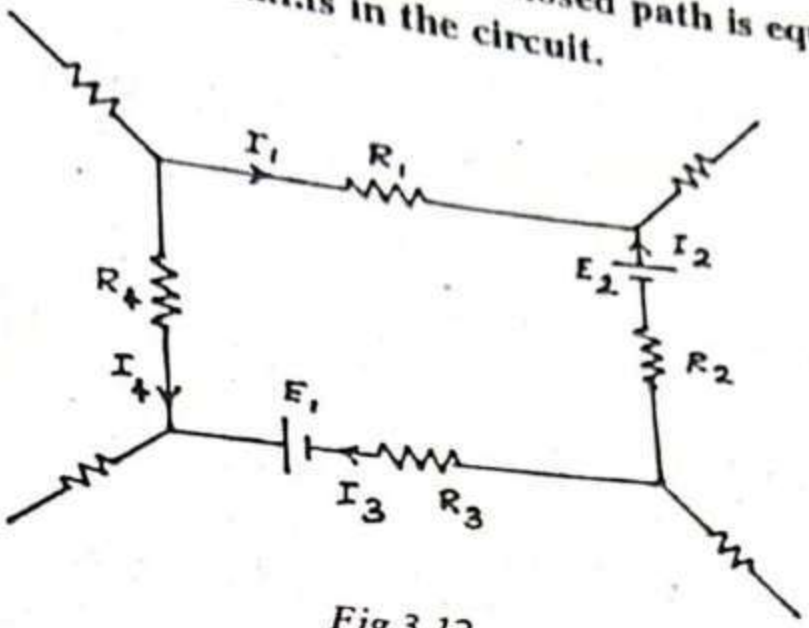

Fig 3.12

Consider a closed loop of circuit ABCDA as shown in fig3-12. In the circuit the current which flows in the clockwise direction is taken as positive and the current which flows in the anticlockwise direction is taken as negative. Also e.m.fs which sents current in the clockwise direction are taken as positive and those that send current in the anticlockwise direction as negative.

Applying Kirchhoff's second law to the circuit in fig3-12, we get

$$I_1 R_1 - I_2 R_2 + I_3 R_3 - I_4 R_4 = E_1 - E_2 \qquad (3)$$

C. Wheatstone Bridge:

Wheatstone bridge consists of four resistances P, Q,R and S connected as shown in fig 3-13. A galvanometer of a resistance G is connected between the points B and D and a cell is connected between the points A and C. Two keys are also connected in the circuit as shown.

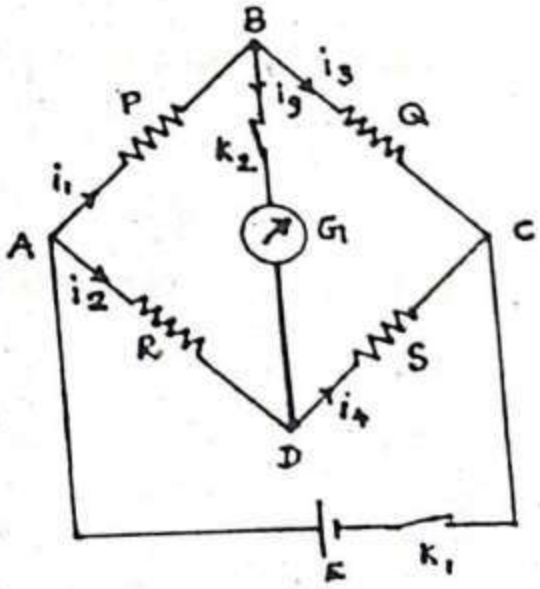

Fig 3.13

When the keys are closed, a current flows in the circuit. Current from the cell is divided into two parts at A.

The current i_1 flows through P and the current i_2 flows through the galvanometer. The current i_3 through Q flows from B to C and the current i_4 through S flows form D to C.

At the junction B, according to Kirchhoff's first law,

$$i_1 - i_g - i_3 = 0 \quad (1)$$

At the junction D, $i_2 - i_g - i_4 = 0 \quad (2)$

The bridge is said to be balanced if there is no flow of current through the galvanometer. For this the resistances are adjusted such that there is no deflection in the galvanometer.

$$\therefore i_g = 0 \quad (3)$$

Hence from equation (1) and (2)

$$i_1 - i_3 = 0 \quad \text{or} \quad i_1 = i_3 \quad (4)$$

$$i_2 - i_4 = 0 \quad \text{or} \quad i_2 = i_4 \quad (5)$$

Applying Kirchhoff's second law to the closed path ABDA, we get

$$i_1P + i_gG - i_2R = 0 \quad (6)$$

In the closed path BCDB,

$$i_3Q - i_4S - i_gG = 0 \quad (7)$$

When $i_g=0$, equation (6) and (7) reduce to

$$i_1P = i_2R \quad (8)$$

$$i_3 Q = i_4 S \quad (9)$$

Dividing the equations (8) and (9) we get

$$\frac{i_1 P}{i_3 Q} = \frac{i_2 R}{i_4 S}$$

But $i_1 = i_3$ and $i_2 = i_4$

$$\therefore \frac{P}{Q} = \frac{R}{S} \quad (10)$$

This is the condition of a balanced Wheatstone bridge. If the value of the resistances P,Q and R are known , the value of S can be calculated. Thus the principle of Wheatstone's bridge is used for the determination of unknown resistances. Metre Bridge, Post office Box and Carey Foster's Bridge work on this principle.

d. Carey Foster's Bridge

Carey Foster's Bridge is the improved form of Metre Bridge. It is more sensitive. Using this, we can determine the difference between two nearly equal resistances. If the value of one resistance is known, the value of the other can be calculated. In this, end resistances are eliminated in calculation. This bridge can also be used to measure accurately a given very low resistances.

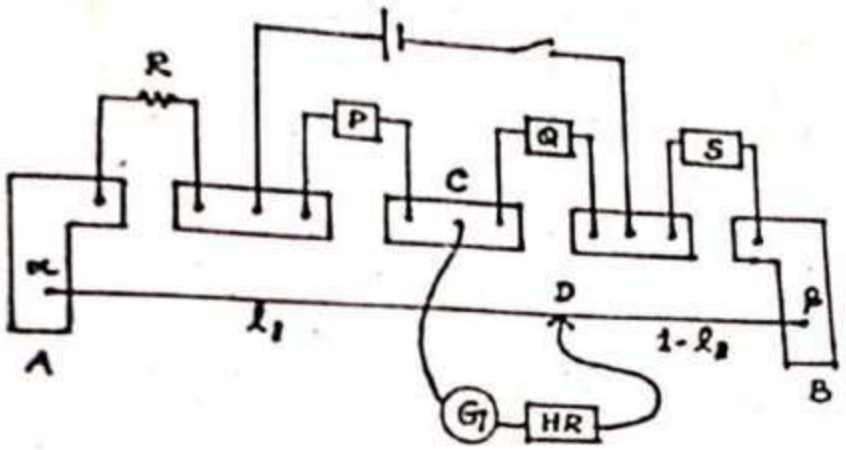

Fig 3-14

It consists of a straight uniform wire of manganin exactly one metre long (AB). The wire is stretched on a wooden board. The ends A and B are joined to thick copper strips of low resistance as shown is fig 3-14. Between in these two copper strips, three copper strips are fixed such that there are four gaps in the wooden board. A meter scale is fixed on the board parallel to the wire.

Two equal resistance P and Q are connected in the inner gaps and the resistances R and S are connected in the outer gaps. The cell and galvanometer are connected as shown in fig. Using a jockey,. contact can be made at any point on the wire AB.

Let α and β be the end resistances at the ends A and B respectively. Let ρ be the resistance per unit length. The resistance R is in left

gap and S in the right gap. Now let l_1 be the balancing length. In this condition, the equivalence Wheatstone bridge is as shown in fig 3-15 When the bridge is balanced.

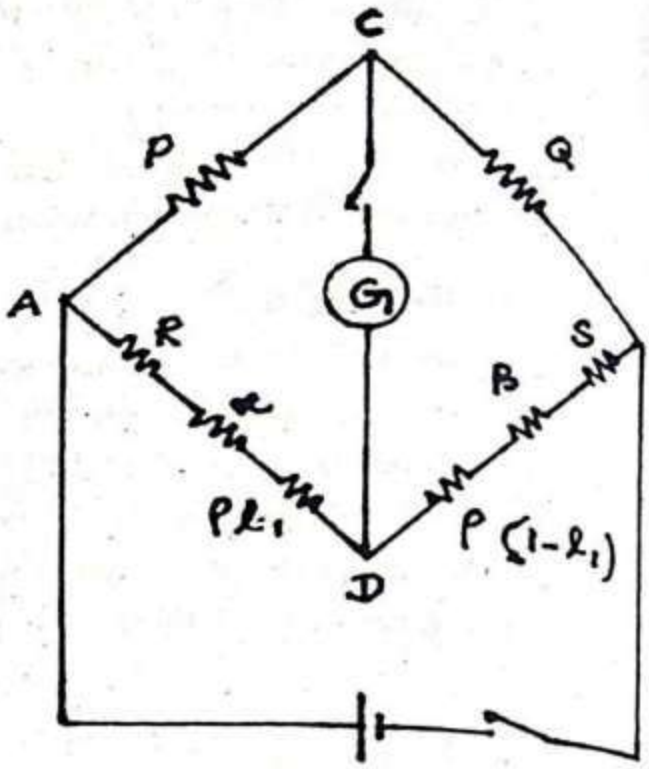

Fig 5.15

$$\frac{P}{Q} = \frac{R + \alpha + l_1 \rho}{S + \beta + (1 - l_1)\rho} \quad (1)$$

Now R and S are interchanged and let the balancing length be l_2.

$$\therefore \frac{P}{Q} = \frac{S + \alpha + l_2 \rho}{R + \beta + (1 - l_2)\rho} \quad (2)$$

Comparing equation(1) and (2) we get

$$\frac{R + \alpha + l_1 \rho}{S + \beta + (1 - l_1)\rho} = \frac{S + \alpha + l_2 \rho}{R + \beta + (1 - l_2)\rho} \quad (2)$$

Adding 1 on both side, we get

$$\frac{R + \alpha + l_1\ \rho + S + \beta + (1 - l_1)\rho}{S + \beta + (1 - l_1)\rho} =$$

$$\frac{S + \alpha + l_2\ \rho + R + \beta + (1 - l_2)\rho}{R + \beta + (1 - l_2)\rho}$$

$$\therefore \frac{R + S + \alpha + \beta + \rho}{S + \beta + (1 - l_1)\rho} = \frac{R + S + \alpha + \beta + \rho}{R + \beta + (1 - l_2)\rho} \quad (4)$$

$$\therefore S + \beta + (1 - l_1)\rho = R + \beta + (1 - l_2)\rho$$

or $$S - l_1 \rho = R - l_2 \rho$$

$$\therefore R - S = \rho(l_2 - l_1)$$

$$\therefore R = S + \rho(l_2 - l_1) \quad (5)$$

Knowing ρ, l_1 and l_2, (R – S) can be calculated.If S is known, R can be calculated.

Determination of ρ*:*

To determine the resistance per unit length of the bridge wire, the resistance R is replaced by a copper strip (R = 0). Now we have to find the balancing length and let it be l_1'. Now keeping S in the left gap and copper strip in the right gap, we have to find the balancing length. Let it be l_2' The values of P and Q should be equal.

$$R = S + \rho(l_2' - l_1')$$

Here $R = 0$

$$\therefore \rho = \frac{S}{(l_1' - l_2')}$$

The experiment is repeated for different values of S. The mean value of ρ is calculated. Using the value of ρ in equation (5), the resistance R can be calculated.

3. POTENTIOMETER

Potentiometer is a device which is used to measure potential difference accurately. It is also used to measure current.

Construction: It consists of ten segment of a uniform wire of magnanin or constantan, each one metre long. The segments are stretched parallel to each other on a horizontal wooden board. The ends of the wires are connected to copper strips of zero resistance. The ends are fitted with binding screws for connection. Using a movable jockey contact can be made at any point of the wire. A metre scale is fixed on the wooden board parallel to the segment of the wire.

Principle of potentiometer:

The principle of the potentiometer can be explained using the circuit shown in fig 3-16. In the figure AB represents the wire of the potentiometer. A and B are connected to a battery of steady emf. When the key in this circuit is closed a steady current flows through the wire of the potentiometer. This circuit is called the primary circuit.

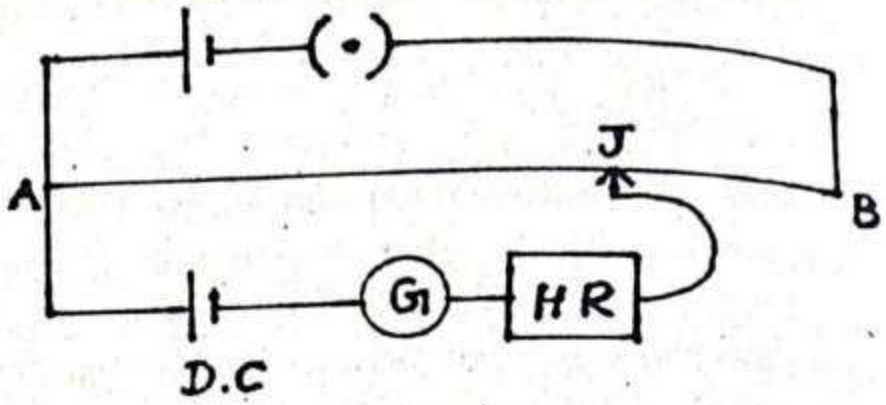

Fig 3-16.

The positive end of the Daniel cell is connected to the end A of the potentiometer. The negative end is connected to the jockey through a high resistance and a galvanometer. This circuit is called the secondary circuit. The positive end of cell is connected to the end A. Hence the current due to this circuit flows in a direction opposite to that of the current due to the primary circuit. Hence the e.m.f of the cell opposes the p.d between the ends of the potentiometer wire, when the jockey makes contact at any point of the wire.

Using the jockey, let the contact be made at the point J on the potentiometer. If the p.d between the points A and J is greater than the e.m.f of the cell in the secondary, the deflection of the galvanometer will be in the righthand side. On the otherhand, if the p.d between the points A and J is less, the deflection will be in the lefthand side. The jockey is moved on the potentiometer wire such that there is no deflection in the galvanometer. In this case the p.d between the point A and the point of contact of jockey on the wire is exactly equal to the e.m.f of the cell in the secondary. In that case the point J is called the balancing point and the length AJ is callled balancing length.. Let the balancing length be l. If i is the current through the potentiometer wire and ρ is the resistance per unit length, the p.d across AJ is $i \rho l$.

If E is the e.m.f of the secondary cell, then

$$E = i \rho l \qquad (1)$$

Since ρ and i are constants,

$$E \propto l \qquad (2)$$

This is the principle of the potentiometer.

a. Measurement of current

For the measurement of current using a potentiometer the circuit is as shown is fig 3-17.

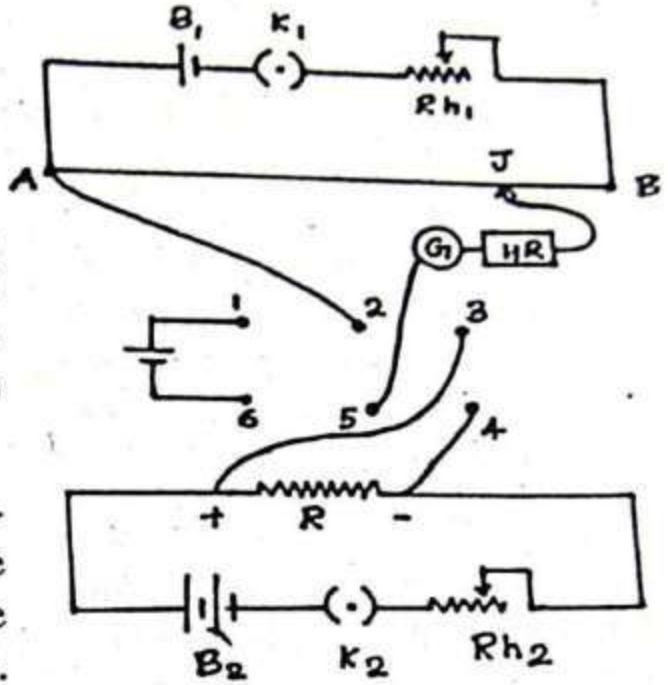

Fig 3.17

The ends of the potentiometer A and B are connected to an accumulator B_1, through a key K_1, and a rheostat Rh_1. This is the primary circuit.

In the secondary, a six terminal key is used. Using this, the two p.d may be included with the potentiometer circuit separately. The middle pair of terminal 2 and 5 are connected to the end A and the jockey through a galvanometer G and a high resistance. A Daniel cell of e.m.f 1.08 volt is connected across the terminals 1 and 6. A battery B_2, key K_2, rheostat Rh_2 and a standard resistance R are connected in series. The positive end of the standard resistance is connected to the terminal 3 and the negative end to 4 as shown in figure.

First including the Daniel cell in the potentiometer, the balancing length is determined. Let the balancing length be l_0. *According to the principle of potentiometer.*

$$1.08 \propto l_o \qquad (1)$$

Next the p.d across the standard resistance R is included in the main circuit and the balancing length l is determined. If i is the current flow through the standard resistance, the p.d across R is i R.

$$\therefore i R \propto l \qquad (2)$$

Dividing equation (2) by equal (1), we get

$$\frac{i R}{1.08} = \frac{l}{l_o} \qquad (3)$$

$$\therefore \quad i = \frac{1.08}{R} \cdot \frac{l}{l_o} \qquad (4)$$

Using equation (4), the current in the circuit can be calculated.

b. Measurement of resistance

To compare the given two resistances, the circuit is as shown in fig 3-18. If one of the resistance is known, the other resistance can be calculated.

In the secondary circuit, a six terminal key is used. Using this, the two p.d may be included with the potentiometer separately. The middle pair of the terminals 2 and 5 are connected to the end A and jockey through a galvanometer and high resistance.

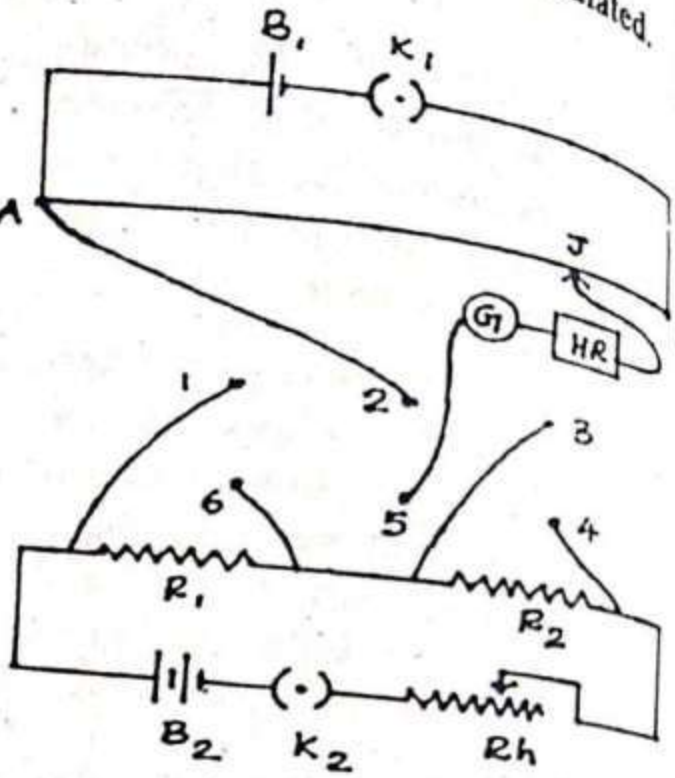

Fig 3.18

Two resistances R_1 and R_2 which are to be compared are connected in series with a battery B_2, key K_2 and a rheostat Rh. The ends of the resistances R_1 and R_2 are connected to the six terminal key as shown in fig. When the key K_2 is closed, a steady current i flows through the resistances R_1 and R_2. The p.d across them will be $i R_1$ and $i R_2$.

First the p.d across R_1 is included in the potentiometer circuit and the balancing length is found. Let it be l_1. According to the principle of potentiometer,

$$i R_1 \propto l_1 \qquad (1)$$

Next the p.d across R_2 is included and the balancing length is found. Let it be l_2.

$$\therefore \quad i R_2 \propto l_2 \qquad (2)$$

Dividing equation (1) by (2) we get

$$\frac{R_1}{R_2} = \frac{l_1}{l_2} \qquad (3)$$

By changing the current in the secondary the experiment is repeated. For each current R_1/R_2 is calculated as described above. Then the mean value of R_1/R_2 is calculated.

If one of the resistance is known, the other can be determined using relation $R_1/R_2 = l_1/l_2$. If R_1 is known, the resistance R_2 can be calculated using the relation.

$$R_2 = R_1 \cdot \frac{l_2}{l_1} \qquad (4)$$

c. Calibration of low range voltmeter

The ends of the potentiometer A and B are connected to a battery of steady e.m.f. The positive end of the Daniel cell is connected to the end A and the negative to the jockey through a galvanometer and a high resistance. Now the balancing length is found. Let it be l_o. The fall of potential per unit length of the potentiometer wire is $1.08/l_o$ volt.

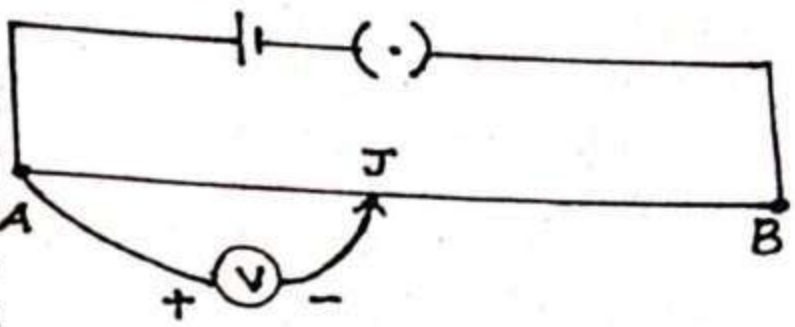

Fig 3.19

The secondary circuit is replaced by a voltmeter. The positive end of the voltmeter is connected to the end A and the negative to the jockey (fig 3-19). The jockey is pressed along the wire so that the voltmeter gives a reading V volt. The length of the wire AJ is found. Let it be l. The p.d between A and J is equal to $\frac{1.08}{l_o} \times l$ volt.

$$\therefore \text{ correction} = \left(\frac{1.08}{l_o} l - V\right)$$

The experiment may be repeated for different value of the voltmeter such as 0.1,0.2....etc. For each voltmeter reading correction

may be calculated. By taking the voltmeter reading along the x- axis and correction along Y-axis , a calibration graph may be drawn.

d. Calibration of a high range voltmeter

An accumulator of steady e.m.f is connected to the ends A and B of the potentiometer, through a key and rheostat. In the secondary by connecting a cell of e.m.f E, the balancing length is found. Let it be l_o. Hence the fall of potential per unit length is E/l_o.

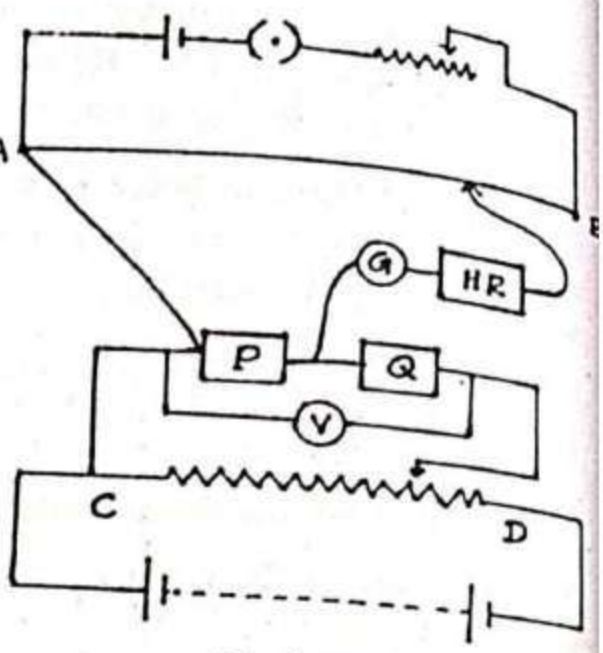

Fig 5.20

For the calibration of high range voltmeter, the circuit is as shown in fig 3-20. The primary is the same that used in the above.

A high D.C Voltage source is connected to the end C and D of a high resistance rheostat. The resistance boxes P and Q are connected in series and one end of it is connected to the slider arm of the rheostat and the other end is connected to the slider arm of the rheostat. The high range voltmeter which is to be calibrated is connected across the ends of P and Q. By moving the slider arm, the desired p.d can be tapped. This arrangement is called the potential divider arrangement. The p.d is measured by the voltmeter.

Resistance of 100 ohm and 9900 ohms are included in P and Q respectively. Hence the potential difference across P is $\frac{P}{P+Q} = \frac{1}{100}$.

It is required that (P + Q) is made very large so that only a small current flows through the resistance boxes even though a high potential is applied between these ends.

By adjusting the rheostat, the voltmeter is made to read V volt and the balancing length is found. Let it be l. Now the p.d across the

end of P is equal to El/l_o. Hence the total p.d at the end P and Q is equal to $\left(\frac{P+Q}{P} \times \frac{El}{l_o}\right)$ volt. But the voltmeter reading is V.

$$\therefore \text{Correction} = \left[\frac{P+Q}{P} \cdot \frac{El}{l_o} - V\right]$$

The experiment is repeated for different values of the voltmeter such as 5, 10, 15 .... etc. For each voltmeter reading, the correction may be calculated and a calibration graph may be drawn.

Scanned Books:

1. V.Vijayendran, 2012, Digital Fundamentals - K.Viswanathan (Printers & Publishers) PVT. LTD., Chennai-31.

2. A.Sundaravelusamy, 2015, Applied Physics Paper I -Priya Publications, Karur-2.