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Department of Physics

APPLIED PHYSICS - I

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APPLIED PHYSICS – I

UNIT-V SEMICONDUCTOR MEMORIES

Introduction-ROM-Using Diodes & Transistors-ROM in terms of digital circuits-Building memory of larger capacity-PROM-EPROM-EEPROM-ROM as a unit in microcomputers-RAM-Static RAM-Dynamic RAM.

Semiconductor memory

Semiconductor memory is used in any electronics assembly that uses computer processing technology. Semiconductor memory is the essential electronics component needed for any computer based PCB assembly.

In addition to this, memory cards have become commonplace items for temporarily storing data - everything from the portable flash memory cards used for transferring files, to semiconductor memory cards used in cameras, mobile phones and the like.

The use of semiconductor memory has grown, and the size of these memory cards has increased as the need for larger and larger amounts of storage is needed.

Semiconductor Memory Classification

<table>
<tr><td colspan="2">Non-Volatile Memory</td><td colspan="2">Volatile Memory</td></tr>
<tr><td>Read Only Memory (ROM)</td><td>Read/Write Memory (RWM)</td><td colspan="2">Read/Write Memory</td></tr>
<tr><td rowspan="2">Mask-Programmable ROM
Programmable ROM</td><td rowspan="2">EPROM
E²PROM
FLASH</td><td>Random Access</td><td>Non-Random Access</td></tr>
<tr><td>SRAM
DRAM</td><td>FIFO
LIFO
Shift Register</td></tr>
</table>

EPROM - Erasable Programmable ROM

E²PROM - Electrically Erasable Programmable ROM

SRAM - Static Random Access Memory

DRAM - Dynamic Random Access Memory

FIFO - First-In First-Out

LIFO - Last-In First-Out

A variety of different memory technologies are available - each one suited to different applications.. Names such as ROM, RAM, EPROM, EEPROM, Flash memory, DRAM, SRAM, SDRAM, as well as F-RAM and MRAM are available, and new types are being developed to enable improved performance.

In addition to this the semiconductor devices are available in many forms - ICs for printed board assembly, USB memory cards, Compact Flash cards, SD memory cards and even solid state hard drives. Semiconductor memory is even incorporated into many microprocessor chips as on-board memory.

Semiconductor memory: main types

There are two main types or categories that can be used for semiconductor technology. These memory types or categories differentiate the memory to the way in which it operates:

RAM - Random Access Memory:

As the names suggest, the RAM or random access memory is a form of semiconductor memory technology that is used for reading and writing data in any order - in other words as it is required by the processor. It is used for such applications as the computer or processor memory where variables and other stored and are required on a random basis. Data is stored and read many times to and from this type of memory. Random access memory is used in huge quantities in computer applications as current day computing and processing technology requires large amounts of memory to enable them to handle the memory hungry applications used today.

ROM - Read Only Memory:

A ROM is a form of semiconductor memory technology used where the data is written once and then not changed. In view of this it is used where data needs to be stored permanently, even when the power is removed - many memory technologies lose the data once the power is removed. As a result, this type of semiconductor memory technology is widely used for storing programs and data that must survive when a computer or processor is powered down. For example the BIOS of a computer will be stored in ROM. As the name implies, data cannot be easily written to ROM. Depending on the technology used in the ROM, writing the data into the ROM initially may require special hardware. Although it is often possible to change the data, this gain requires special hardware to erase the data ready for new data to be written in.

Each of the semiconductor memory technologies outlined below falls into one of these two types of category. each technology offers its own advantages and is used in a particular way, or for a particular application.

EEPROM:

This is an Electrically Erasable Programmable Read Only Memory. Data can be written to these semiconductor devices and it can be erased using an electrical voltage. This is typically applied to an erase pin on the chip. Like other types of PROM, EEPROM retains the contents of the memory even when the power is turned off. Also like other types of ROM, EEPROM is not as fast as RAM.

EPROM:

This is an Erasable Programmable Read Only Memory. These semiconductor devices can be programmed and then erased at a later time. This is normally achieved by exposing the semiconductor device itself to ultraviolet light. To enable this to happen there is a circular window in the package of the EPROM to enable the light to reach the silicon of the device. When the PROM is in use, this window is normally covered by a label, especially when the data may need to be preserved for an extended period.

The PROM stores its data as a charge on a capacitor. There is a charge storage capacitor for each cell and this can be read repeatedly as required. However it is found that after many years the charge may leak away and the data may be lost.

Flash memory:

Flash memory may be considered as a development of EEPROM technology. Data can be written to it and it can be erased, although only in blocks, but data can be read on an individual cell basis.

To erase and re-programme areas of the chip, programming voltages at levels that are available within electronic equipment are used. It is also non-volatile, and this makes it particularly useful. As a result Flash memory is widely used in many applications including USB memory sticks, compact Flash memory cards, SD memory cards and also now solid state hard drives for computers and many other applications.

PROM:

This stands for Programmable Read Only Memory. It is a semiconductor memory which can only have data written to it once - the data written to it is permanent. These memories are bought in a blank format and they are programmed using a special PROM programmer. Typically a PROM will consist of an array of fuseable links some of which are "blown" during the programming process to provide the required data pattern.

SRAM:

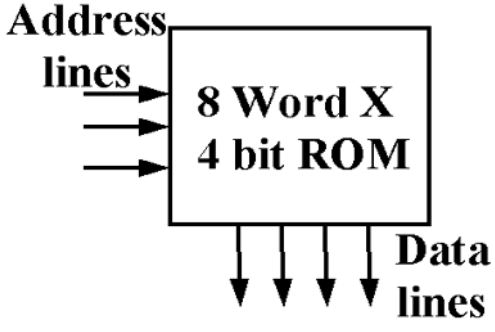
Static Random Access Memory. This form of semiconductor memory gains its name from the fact that, unlike DRAM, the data does not need to be refreshed dynamically.

These semiconductor devices are able to support faster read and write times than DRAM (typically 10 ns against 60 ns for DRAM), and in addition its cycle time is much shorter because it does not need to pause between accesses. However they consume more power, they are less dense and more expensive than DRAM. As a result of this SRAM is normally used for caches, while DRAM is used as the main semiconductor memory technology.

DRAM:

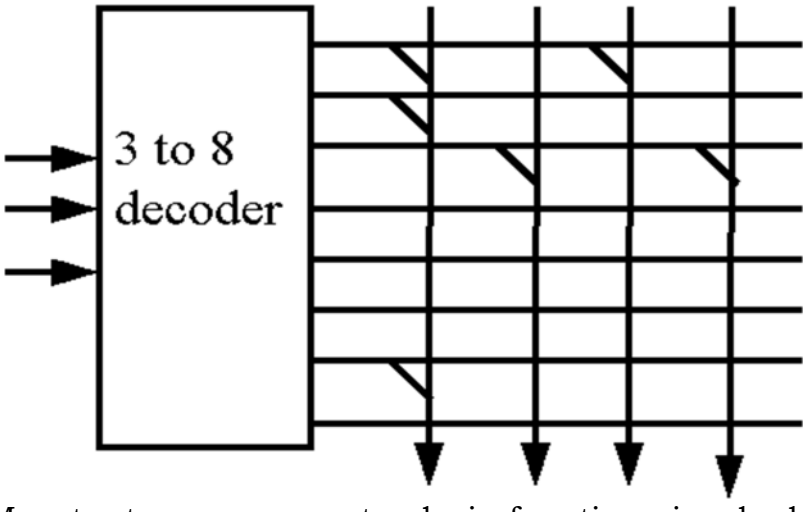
Dynamic RAM is a form of random access memory. DRAM uses a capacitor to store each bit of data, and the level of charge on each capacitor determines whether that bit is a logical 1 or 0. However these capacitors do not hold their charge indefinitely, and therefore the data needs to be refreshed periodically. As a result of this dynamic refreshing it gains its name of being a dynamic RAM. DRAM is the form of semiconductor memory that is often used in equipment including personal computers and workstations where it forms the main RAM for the computer. The semiconductor devices are normally available as integrated circuits for use in PCB assembly in the form of surface mount devices or less frequently now as leaded components.

Read Only Memories (ROM)



- once data is stored in ROM it can be read out , but stored data cannot be changed
- ROM with n bits input lines, and m bits output lines contains array of 2^n words, each is m bits long
- when input combination is applied to ROM, the word (pattern of 0's 1's) which is stored at that input combination address appears at the output lines
- 2^n X m ROM can realize m functions of n variables
- ROM consists of decoder and memory array
- multiple output combinational networks can easily be realized using ROMs
- Example
    - mask programmable: data defined during manufacture process (mask identifies presence of switching elements)
    - field -programmable PROM: connection of switching element to wordline done by user using fusible links
    - erasable programmable EPROM: charge storage is used to enable or disable switching elements in the array. can be erased by UV light. Note EEPROM uses electrical pulses instead of UV light electrically erasable PROM

- ROM consists of a address decoder and memory array. For example in diagram below address 0000 stores 1010.



- each ROM output can represent a logic function signal whose truth table is stored in the ROM. e.g. at address a,b,c,d = 0000 the lsb of the stored word represents logic function f(a,b,c,d)=f(0,0,0,0), etc... In this example the lsb of ROM output word generates the logic function f(a,b,c,d), with ROM address a,b,c,d.

Read Only Memory

Read-only memory (ROM) is just that: memory that can only be read from, not written to. Some forms are can be written, but only by using special tools.

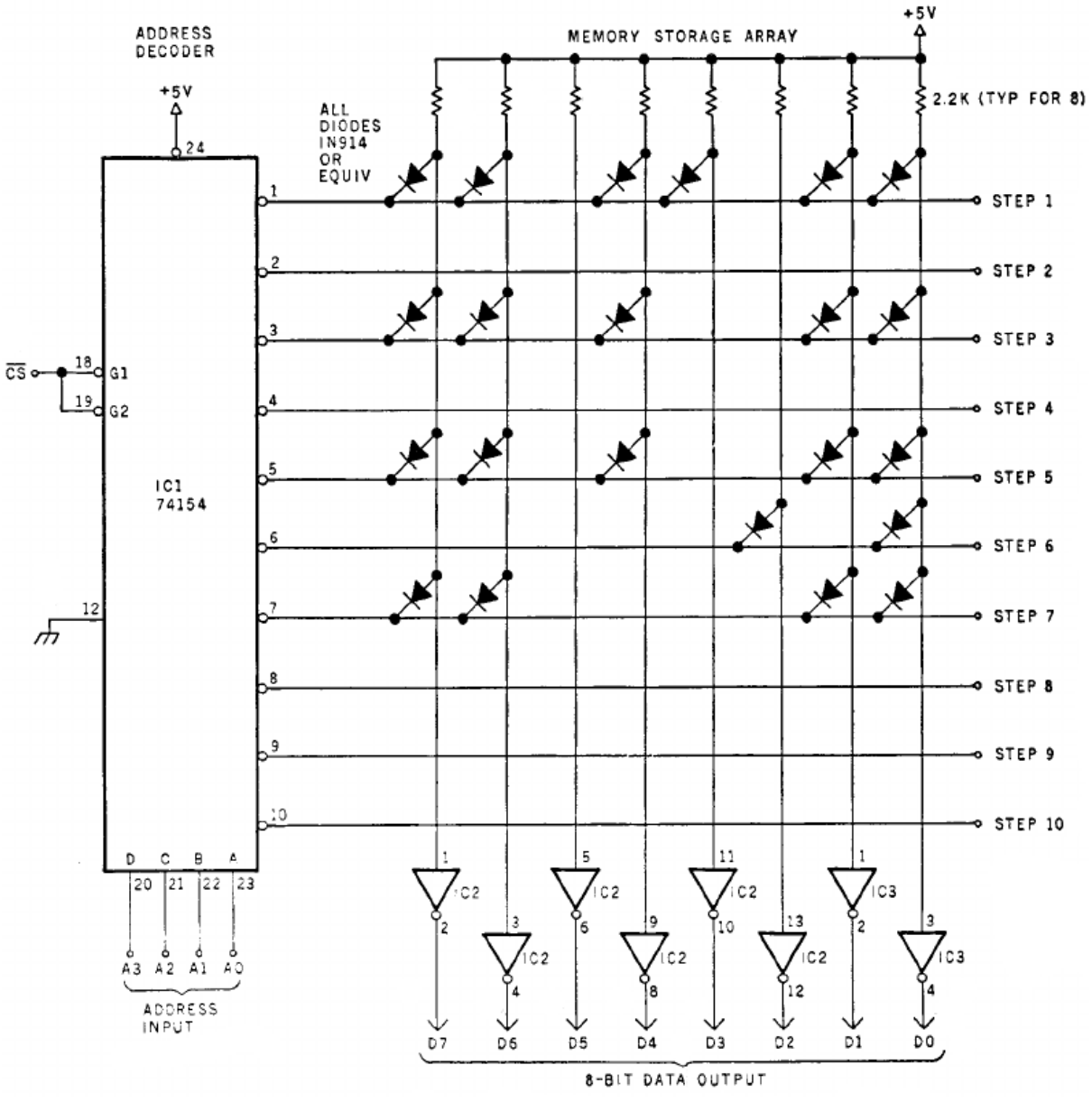
Mask ROM

This goes all the way back to the dawn of semiconductor technology. This is basically one big lookup table that is designed into the chip. As such there is no programmability once the chips are made. To change the contents, the circuit is changed and new chips are manufactured. This has several downsides:

1. It is only financial feasible to do in large quantities.
2. Any updates involve a product recall/update/return.
3. Time from design to part is long due to the manufacturing timeline.
4. Unusable for experimenting or small batches.

The circuit involved has several input lines, typically decoded from a binary encoded address, and whatever number of output lines are required, The input lines are connected to the output lines, or not, by a diode to encode the data at each address. The following is a small, simple implementation of ROM. It's not a mask ROM, but is an implementation of the same approach. The 74154 is an 8-to-16 decoder, much like the 3-to-8 decoder we saw in an early part of this guide (the 74138). Only the first few (of 16) addresses are shown, for brevity. The output corresponding to the address A (bottom left) goes low, while the rest remain high. The pullups at the top

ensure that outputs are normally high. When an output of the '154 goes low (its address is on the A inputs and the /CS input is low) any output line connected to it through a diode goes low. In this way we can read the byte at any of the 16 locations. Note the inverters on the output lines, this negates the sense of the bits, resulting in a 1 wherever there is a diode. For example, at address 0 (the '154 output labelled "1") the data is 11011011.



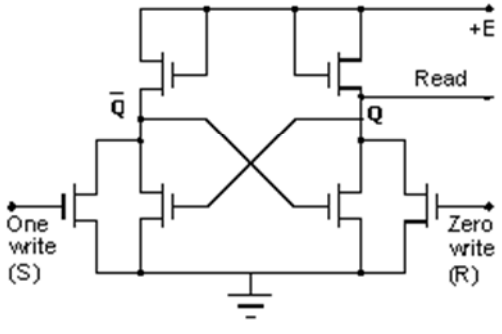
Static RAM memories

Static RAM memory cells are built as static RS flip-flops based on bipolar or MOS transistors. The structure of a basic memory bit cell built with MOS transistors (without control) is shown below. The cell is built of 6 MOS transistors that are coupled to create a static RS flip-flop. To each bit flip-flop, a row select line has to be attached. In a stable state, the Q output is in the

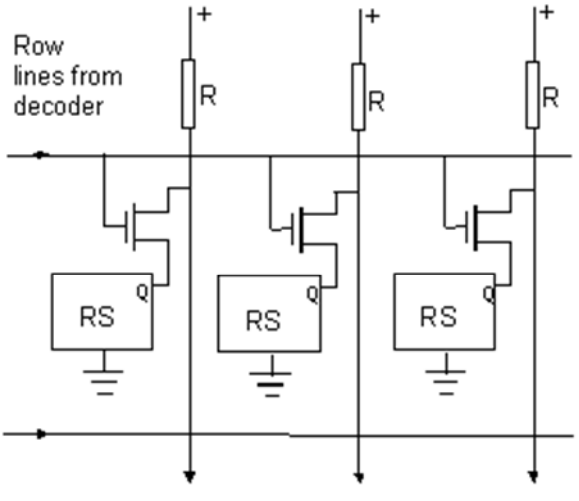
state 0 (0V) and the "not-Q" output is in the state1 (+EV). Inserting 1 at S input makes the flip-flop enter an opposite state, for which the Q output shows 1. Inserting 1 at R input makes the flip-flop take the 0 state with 0 at Q output.

Such flip-flops are inserted at intersections of row select lines and output signal column lines in a matrix of memory cells, similar to that which appeared in the ROM memory. Each flip-flop stores one bit of a word written in a row. Outputs Q of all flip-flops in a row are connected to output column lines by means of control transistors, which are opened by signal from the row line. If a given row is selected, all flip-flops that are in the state 0, output this state to the column lines through control transistors. For flip-flops in the state 1, the control transistors will not be opened and the column lines will remain in the state 1. In a similar way, the write lines for "zeros" and "ones", which go perpendicularly in columns, are connected to all bit cells in the memory, through transistors which are opened by signals from row lines.

A schematic of these connections can be easily drawn as an exercise to this lecture.



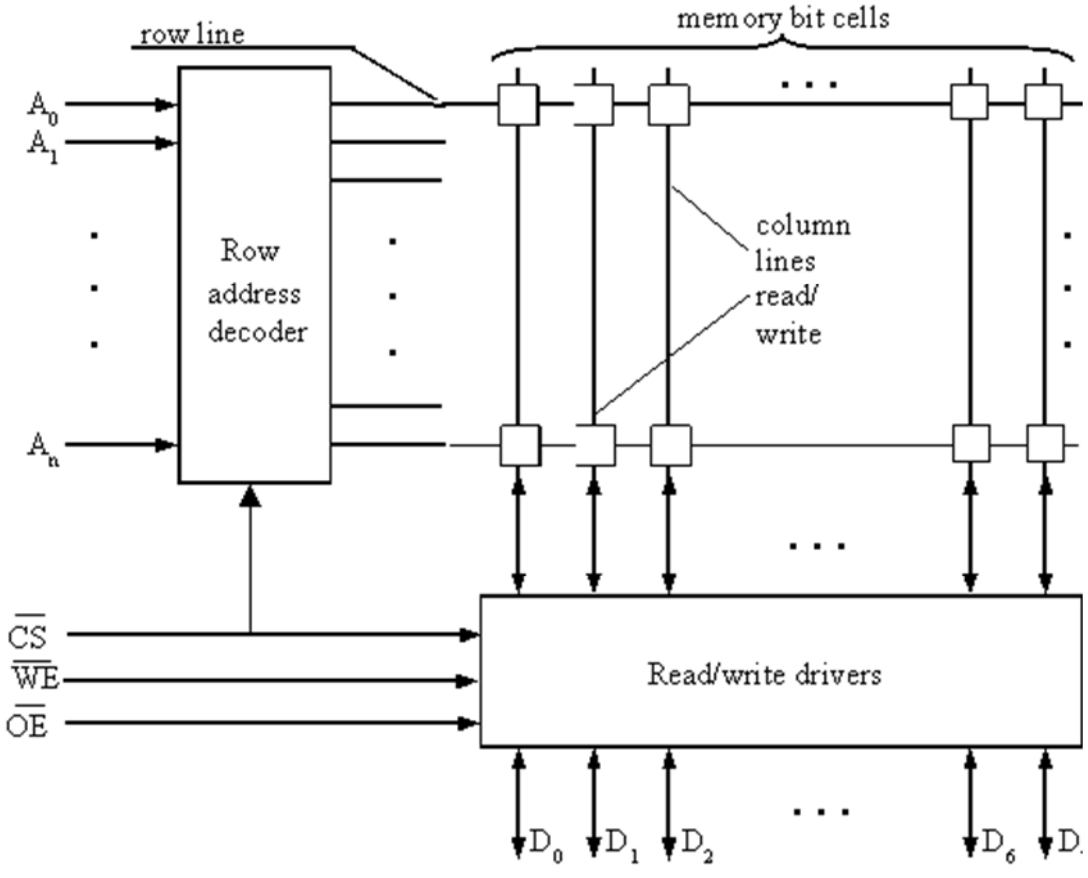
SRAM memory bit cell



To SRAM memory output

SRAM memory internal structure based on MOS transistors: bit cell and bit read control

A block diagram of a SRAM memory module with 8-bit word is shown below. We can see the pins to which address bits are supplied - A_1 - A_n, data on write and read - D_0 - D_7 (the same pins are used for this) and control signals: the memory module select signal - CS (from Chip Select), the signal that opens data input on write - WE (from Write Enable), the signal which opens data output on read - OE (from Output Enable). The CS signal is generated on the basis of decoding of the most significant address bits done outside the memory module.

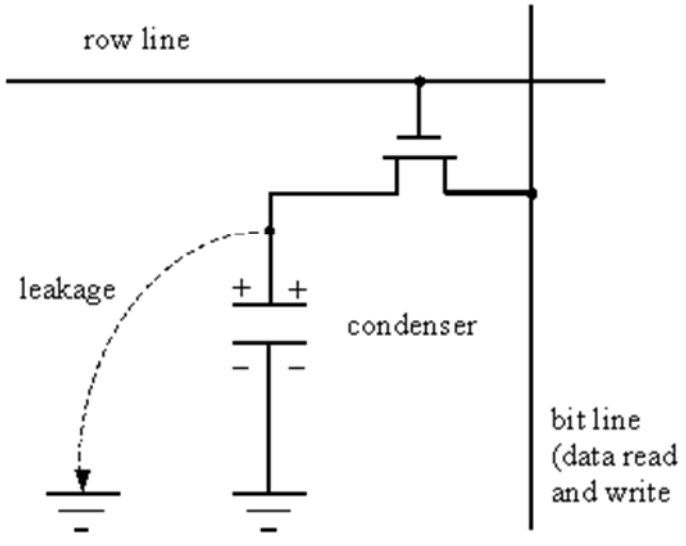


Block diagram of a SRAM memory module

Dynamic RAM memories

Bit cells of the dynamic RAM memory are built based on the electric charge storing in condensers. A bit cell constitutes a transistor with a condenser interconnected to the line that selects a memory row and to the bit line in the word (bit read and write lines). The figure below shows such a bit cell based on MOS transistor. A write takes place as a result of row line selection (positive voltage) and insertion through a bit line of the voltage that corresponds to the stored bit: 0V for logical zero and the positive voltage for one. For logical one, the condenser will charge through the conducting transistor to the positive voltage. For zero, the transistor will be turned off and the condenser will discharge if loaded or it will remain not charged (in both cases the condenser plate at the transistor side will reach 0V potential). On read, a row line will be set to the positive potential and the transistor will be turned on. If the condenser was charged (the bit cell was storing one), the positive voltage from the condenser plate will be transferred into the bit line (readout of one) after which the condenser discharges through the bit line. If the condenser was not charged, 0V will be transferred to the bit line i.e. a logical zero, stored in this cell. After readout of a bit cell, the condenser has to be charged again to restore the previous contents of the memory cell. It is done by execution of the read cycle for the same information. As we can see, a data readout from

dynamic RAM memory is destructive and in this memory a read cycle is always followed by a write cycle.



Structure of a dynamic RAM bit cell

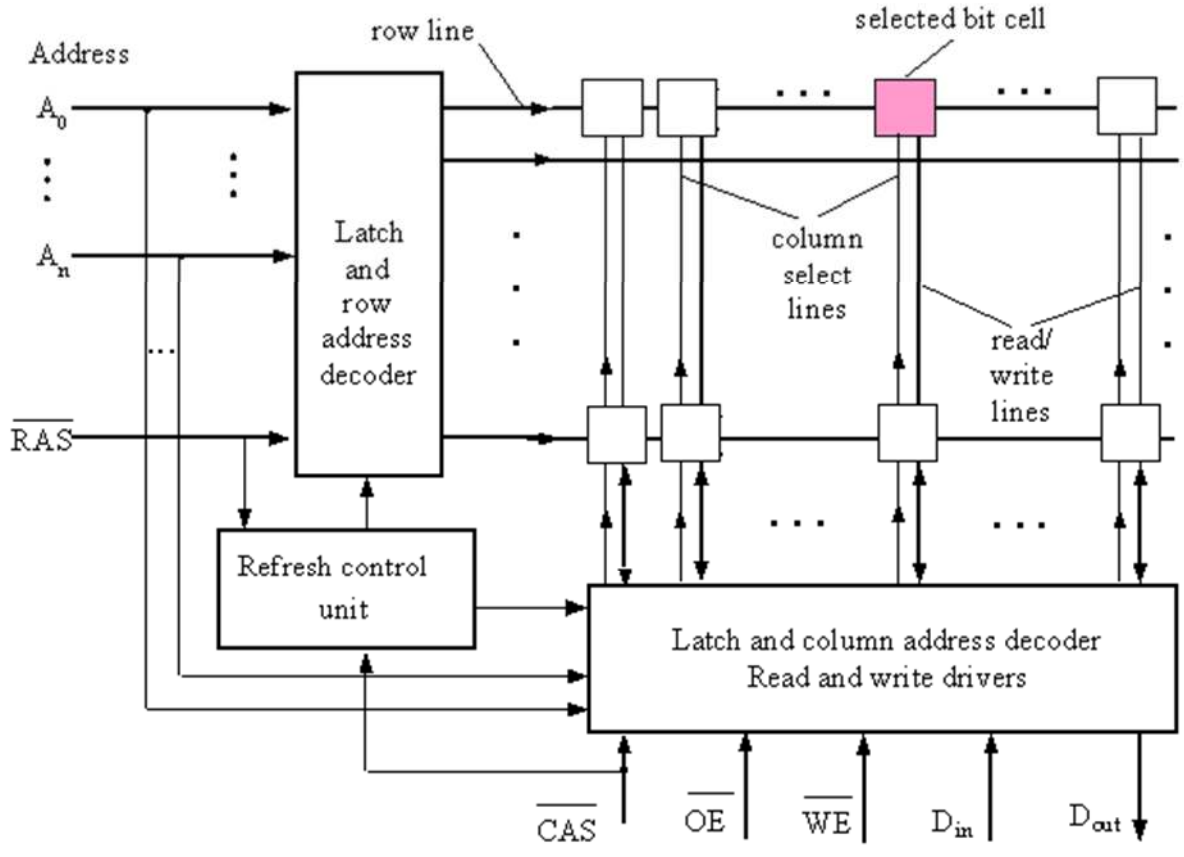
A semiconductor dynamic RAM memory is a volatile memory, since charged condensers are subject to spontaneous discharging. The reason for this is the leakage that results from impurities in the crystalline structure of silicon. Therefore, dynamic RAM memory requires periodic refreshing of stored data. This is done by special refresh circuits, which are always added as an extension of the proper data storing circuitry.

Dynamic RAM

Semiconductor dynamic RAM memories (**DRAMs)** are built using several techniques. The oldest one, which is not currently used is the asynchronous technique. With this technique, the memory works in asynchronous manner in respect to the processor, i.e. memory access is not synchronized by processor clock.

This type of memory is called **Page Mode DRAM,** from calling a row of the memory a page in memory designers jargon. A block diagram of a module of the asynchronous DRAM memory is shown below. This memory has two dimensional cell selection by the use of row and column lines. Bit cells are organized in plates, which correspond to successive bit positions in the memory word. Word address is divided into row and column addresses, which are sent to the memory module in the multiplexed way i.e. sequentially with the use of the same address bus. The row and column addresses are first latched in buffer registers that co-operate with row and column address decoders. The module includes also a control unit. Refreshing is done by rows

of bit cells. During refreshing, access from the processor side and memory output to processor are blocked. The refreshing is done each several to several tens of milliseconds.



Block diagram of a DRAM memory module

In an asynchronous DRAM memory, the pins have the following use: $\mathbf{A_0}$-$\mathbf{A_n}$ - row and column addresses, **RAS** (from Row Address Strobe) - row address identification, **CAS** (from Column Address Strobe) - column address identification, **WE** (from Write Enable) - write control, **OE** (from Output Enable) - read control, $\mathbf{D_{in}}$ - input data line, $\mathbf{D_{out}}$ - output data line. The diagram below presents control signals for the asynchronous dynamic DRAM memory.

UNIT-III

NUMBER SYSTEM, CODES AND LOGIC GATES

Number system-conversions-Binary: Addition, Subtraction, Multiplication, Division-8421 code-BCD code-Excess 3 code-Gray code -Binary to Gray and Gray to Binary Conversion-ASCII code-Basic and Derivative code: AND, OR, NOT, NAND, NOR, EX-OR-NAND & NOR as Universal Gate.

Number systems

A digital computer is a programmable machine that processes binary data I.e., data represented in binary number system. There are methods to convert one number system to another number system. They are

Decimal numbers, Binary numbers, Binary to decimal, Decimal to binary, Hexadecimal number system, Hexadecimal to decimal, Decimal to hexadecimal, Hexa decimal to binary, Binary to hexadecimal, Octal number system, Octal to decimal conversion, Decimal to octal conversion, octal to binary conversion, Binary to octal conversion.

Conversions

(i) Decimal number system

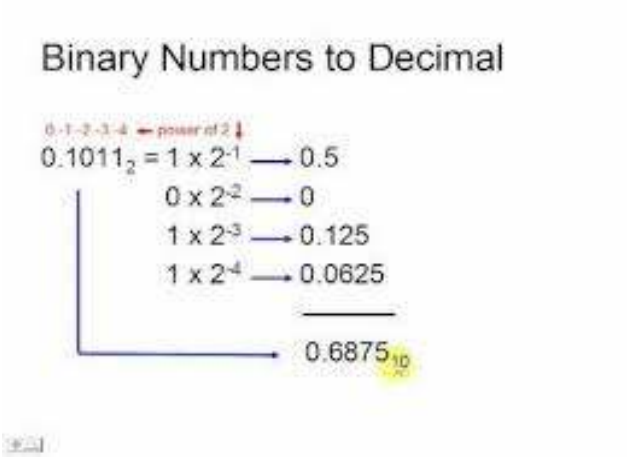
The decimal number system use of Ten digits 1,2,3,4,5,6,7,8,9. Since decimal numbers are said to base or radix of ten. All the digits in the decimal number system expressed in powers of 10,like10^0,10^1, 10^2etc., this is for integer part represents the units tens, hundreds etc., Then for functional part 10^0,10^{-1}, 10^{-2} etc. are called weights.The integer portion and fractional portion in a decimal number system are separated by a decimal point.

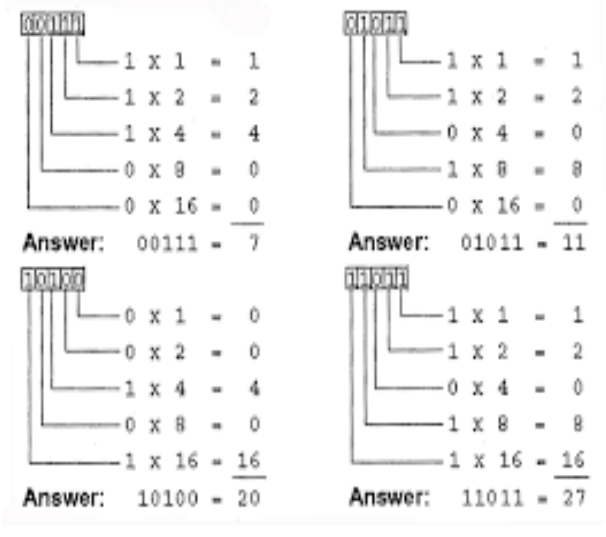
(ii) Binary number system

A binary number system uses only two symbols or digits namely, 0 and 1. Binary numbers have base or radix of 2. Binary digit 0 or 1 is often called a bit. The bits have powers of 2 like 2^0 ,2^1, 2^2 etc., for integer portion and 2^0 ,2^{-1}, $2-^2$ etc., for the fractional part. Then we have decimal point in binary number system.

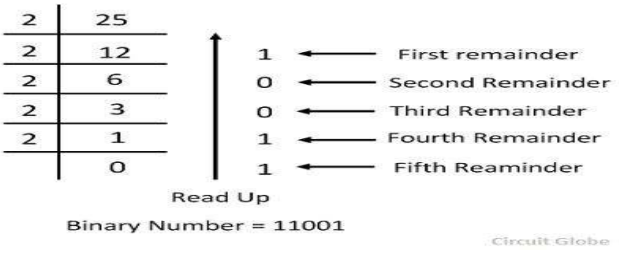
4 bit-nibble,8 bit –byte,16 bit binary word-word and 32-bit double word.

Binary to Decimal conversion





Decimal to Binary

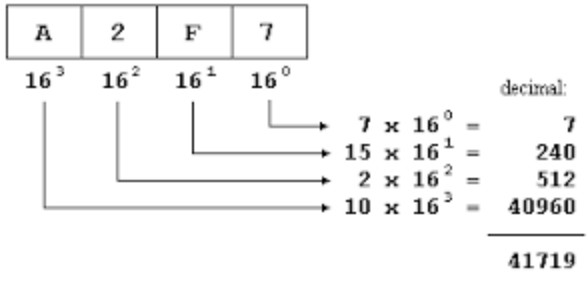


Hexa Decimal numbers system

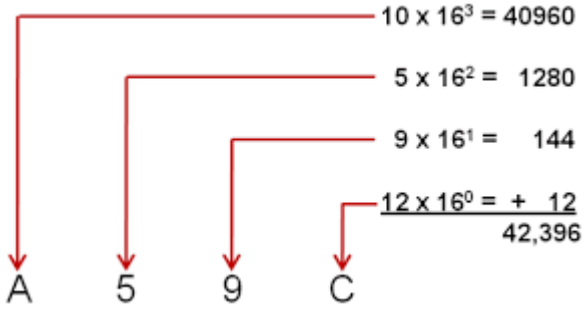
The one main disadvantage of binary numbers is that the binary string equivalent of a large decimal base-10 number can be quite long. When working with large digital systems, such as computers, it is common to find binary numbers consisting of 8, 16 and even 32 digits which makes it difficult to both read or write without producing errors especially when working with lots of 16 or 32-bit binary numbers. numbering system also commonly used

in computer and digital systems called Hexadecimal Numbers. The "Hexadecimal" or simply "Hex" numbering system uses the Base of 16 system. Being a Base-16 system, the hexadecimal numbering system therefore uses 16 (sixteen) different digits with a combination of numbers from 0 through to 15. In other words, there are 16 possible digit symbols. However, there is a potential problem with using this method of digit notation caused by the fact that the decimal numerals of 10, 11, 12, 13, 14 and 15 are normally written using two adjacent symbols. For example, if we write 10 in hexadecimal, do we mean the decimal number ten, or the binary number of two (1 + 0). To get around this tricky problem hexadecimal numbers that identify the values of ten, eleven, . . . , fifteen are replaced with capital letters of A, B, C, D, E and F respectively.

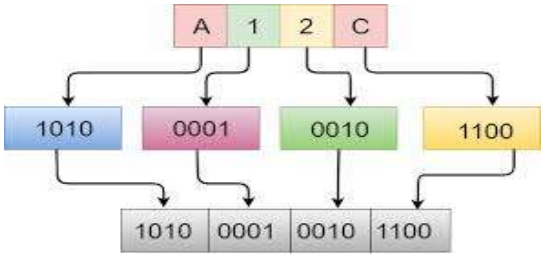
Hexa decimal to decimal



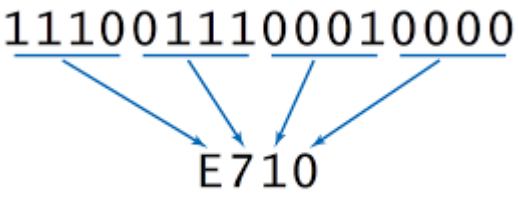
Decimal to hexadecimal



Hexadecimal to Binary



Binary to Hexadecimal



Octal number system

A number system which has its base as 'eight' is called an Octal number system. It uses numbers from 0 to 7. Let us take an example, to understand the concept. As we said, any number with base 8 is an octal number like 248, 1098, 558, etc. Like Octal number is represented with base 8, in the same way, a binary number is represented with base 2, decimal number with base 10 and the hexadecimal number is represented with base 16. Examples for these number systems are:

Octal to Decimal Number

Let us learn here, conversion of Octal number to Decimal Number or base 8 to base 10.

Example: Suppose 2158 is an octal number, then it's decimal form will be,

$2158 = 2 \times 82 + 1 \times 81 + 5 \times 80$

$= 2 \times 64 + 1 \times 8 + 5 \times 1 = 128 + 8 + 5$

$= 14110$

Decimal to Octal Number

Solution: If 560 is a decimal number, then,

560/8=70 and remainder is 0

70/8=8 and remainder is 6

8/8=1 and remainder is 0

And 1/8=0 and remainder is 1

So the octal number starts from MSD to LSD, i.e. 1060

Therefore, $56010 = 10608$

Binary To Octal Number

Solved Example

Example: Convert (100010)2 to octal number.

100→4

and 010→2

Therefore, (100010)2 = 42

A binary number can be converted into an octal number, with the help of the below-given table.

Octal Number to binary and binary to octal from this table

	Binary Equivalent
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Binary arithmetic operations

Binary addition

Rules

A + B	SUM	CARRY
0 + 0	0	0
0 + 1	1	0
1 + 0	1	0
1 + 1	0	1

example

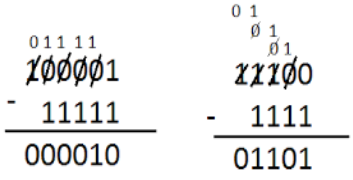
```
  10010        1011101        10011
+ 1100       + 1000000      + 1111101
-------      ---------      ---------
  11110       10011101       10010000

  10011001     11000011       1001100
+   100111   +   101111     + 1100101
----------   ----------     ---------
  11000000     11110010       10110001
```

Binary subtraction

Rules **example**

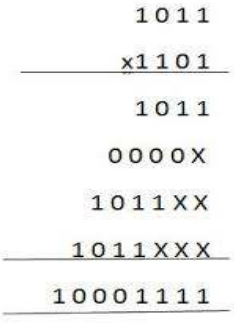
$0-0=0$
$0-1=1$, *borrow 1 from the next more significant bit*
$1-0=1$
$1-1=0$



Binary multiplication

Rules **example**

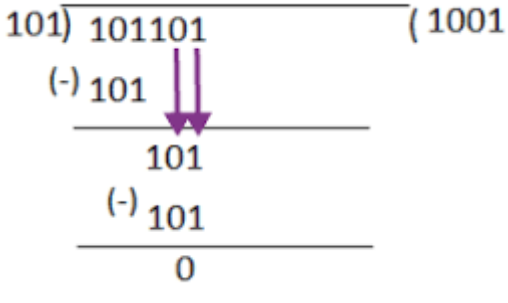
$0\times0=0$
$1\times0=0$
$0\times1=0$
$1\times1=1$(*there is no carry or borrow for this*)



Binary Division

Rules

0/1=0,1/0=1



quotient=1001, remainder=0

8421 code

The BCD8421 code is so called because each of the four bits is given a 'weighting' according to its column value in the binary system. The least significant bit (lsb) has the weight or value 1, the next bit, going left, the value 2. The next bit has the value 4, and the most significant bit (msb) the value 8, as shown in table. So the 8421BCD code for the decimal number 610 is

01108421. Check this from Table. For numbers greater than 9 the system is extended by using a second block of 4 bits to represent tens and a third block to represent hundreds etc.2410 in 8 bit binary would be 00011000 but in BCD8421 is 0010 0100.99210 in 16 bit binary would be 00000011111000002 but in BCD8421 is 1001 1001 0010. BCD is that, because sixteen values are available from four bits, but only ten are used, there are several redundant values whichever BCD system is used. This is wasteful in terms of circuitry, as the fourth bit (the 8s column) is under used. Try some simple conversions between Decimal and BCD 842132110 to BCD8421

6523110 to BCD8421

001101110110 BCD8421 to decimal.

0011001011000110 BCD8421 to decimal.

	MSB	BCD_{8421}		LSB
Decimal	8	4	2	1
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

BCD code

In computing and electronic systems, binary-coded decimal (BCD) is a class of binary encodings of decimal numbers where each digit is represented by a fixed number of bits, usually four or eight. BCD typically encodes two digits within a single byte by taking advantage of the fact that four bits are enough to represent the range 0 to 9. BCD was used in many early decimal computers, and is implemented in the instruction set of machines such as the IBM System/360 series and its descendants, Digital Equipment Corporation's

VAX, the Burroughs B1700, and the Motorola 68000-series processors. BCD per se is not as widely used as in the past and it is no longer implemented in newer computers' instruction sets (e.g. ARM); x86 does not support its BCD instructions in long mode any more. However, decimal fixed-point and floating-point formats are still important and continue to be used in financial, commercial, and industrial computing, where the subtle conversion and fractional rounding errors that are inherent in floating point binary representations cannot be tolerated.

Excess-3 code

Biased codes are a way to represent values with a balanced number of positive and negative numbers using a pre-specified number N as a biasing value. Biased codes (and Gray codes) are non-weighted codes. In excess-3 code, numbers are represented as decimal digits, and each digit is represented by four bits as the digit value plus 3 (the "excess" amount):

The smallest binary number represents the smallest value (0 − excess). The greatest binary number represents the largest value (2N+1 − excess − 1).

Excess-3 arithmetic uses different algorithms than normal non-biased BCD or binary positional system numbers. After adding two excess-3 digits, the raw sum is excess-6. For instance, after adding 1 (0100 in excess-3) and 2 (0101 in excess-3), the sum looks like 6 (1001 in excess-3) instead of 3 (0110 in excess-3). In order to correct this problem, after adding two digits, it is necessary to remove the extra bias by subtracting binary 0011 (decimal 3 in unbiased binary) if the resulting digit is less than decimal 10, or subtracting binary 1101 (decimal 13 in unbiased binary) if an overflow (carry) has occurred. (In 4-bit binary, subtracting binary 1101 is equivalent to adding 0011 and vice versa.)

Decimal	Binay (BCD) 8 4 2 1	Excess-3 Code
0	0 0 0 0	0011
1	0 0 0 1	0100
2	0 0 1 0	0101
3	0 0 1 1	0110
4	0 1 0 0	0111
5	0 1 0 1	1000
6	0 1 1 0	1001
7	0 1 1 1	1010
8	1 0 0 0	1011
9	1 0 0 1	1100

ASCII Code

ASCII abbreviated from American Standard Code for Information Interchange, is a character encoding standard for electronic communication. ASCII codes represent text in computers, telecommunications equipment, and other devices. Most modern character-encoding schemes are based on ASCII, although they support many additional characters. ASCII reserves the first 32 codes (numbers 0–31 decimal) for control characters: codes originally intended not to represent printable information, but rather to control devices (such as printers) that make use of ASCII, or to provide meta-information about data streams such as those stored on magnetic tape.

Logic Gates

We learned is most definitely the basic logic gates and derivatives (AND, OR, XOR, NOT). We looked at their symbols, truth tables and applications in programs. Every logic gate is derived from AND, OR, XOR and NOT.

AND gate

2 Input AND gate		
A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

The AND gate is an electronic circuit that gives a **high** output (1) only if **all** its inputs are high. A dot (.) is used to show the AND operation i.e. A.B. Bear in mind that this dot is sometimes omitted i.e. AB. This represents multiplication between the inputs

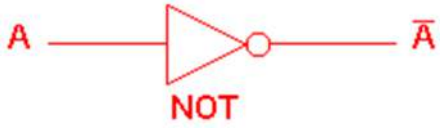
OR Gate

Another basic logic gate we learned during the theory sections of the course is the OR gate which has two inputs which will cause an output so long as either A OR B is 1 (HIGH).

2 Input OR gate		
A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

NOT Gate

Another derivative we learned at the beginning of the semester is the NOT gate which essentially inverts the input as the output. For example, applying a NOT to an OR gate would inverse the outputs of the truth table.



NOT gate	
A	$\overline{A}$
0	1
1	0

XOR Gate

The final derivative we learned during the theory lessons is the XOR gate or the exclusively "OR" gate. This logic gate's truth table is exclusively one input or the other input but not both, making it exclusively OR.

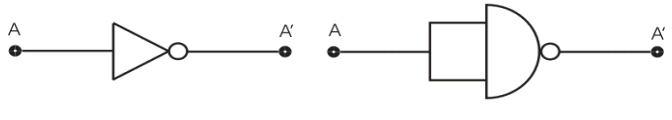
2 Input EXOR gate		
A	B	A⊕B
0	0	0
0	1	1
1	0	1
1	1	0

NAND as a Universal gate

The below diagram is of a two input NAND gate. The first part is an AND gate and second part is a dot after it represents a NOT gate. We will consider the truth table of the above NAND gate i.e. a two-input gate. The two input are A and B.

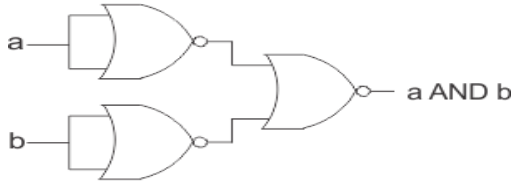
This is the circuit diagram of a NAND gate used to make work like a NOT gate, the original logic

This is the circuit diagram of a NAND gate used to make work like a NOT gate, the original logic gate diagram of NOT g ate is given beside.

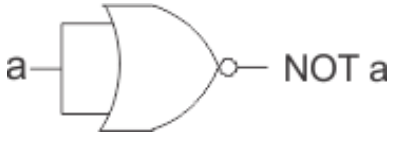


NOR gate as universal gate

We have seen how NAND gate can be used to make all the three basic gates by using that alone. Now we will discuss the same in case of NOR gate. The above diagram is of an OR gate made by only using NOR gates. The output of this gate is exactly similar to that of a single OR gate. As we can see the circuit arrangement of OR gate using NOR gates is similar to that of AND gate using NAND gates.



The above diagram as the name suggests is of AND gate using only NOR gate, again we can see that the circuit diagram of AND gate using only NOR gate is exactly similar to that of OR gate using only NAND gates. Now we will finally see how a NOT gate can be made by using only NOR gates.



The above diagram is of a NOT gate made by using a NOR gate. The circuit diagram is similar to that of NOT gate made by using only NAND gate. So, from the above discussion it is clear that all the three basic gates (AND, OR, NOT) can be made by only using NOR gate. And thus, it can be aptly termed as Universal Gate.

Unit – II: Alternating Current

Root mean square value of an alternating current- average value of an alternating current- alternating EMF applied to a circuit containing L, C, R, L and R, C and R, LCR series and parallel resonance circuits- Q factor

Introduction

- We have already discussed about direct current (DC) which is produced by the voltage source whose pole does not change their polarity with time
- Hence direction of flow of direct current does not changes with time
- Alternating current on the other hand is produced by voltage source whose terminal polarity keeps alternating with time i.e. terminal which was positive at one instant of time becomes negative some time later and vice -versa
- Due to changing polarity of voltage source direction of flow of current also keep changing
- In this chapter we would learn how voltage and current changing with time are related to each other in various circuits with components namely resistors, capacitor and inductor.

Root mean square value of Alternating current and Alternating EMF

- An alternating current is one whose magnitude changes sinusoidal with time .Thus alternating current is given by

$$i = i_0 \sin(\omega t + \phi) \qquad \text{-----(1)}$$

Where i_0=current amplitude or peak value of alternating current
If T is the time period of alternating current and f is the frequency, then

$$\omega = \frac{2\pi}{T} = 2\pi f \qquad \text{-----(2)}$$

Where ω is called angular frequency of A.C and φ is known as phase constant

- Instead of sine function AC can also be represented by cosine function and both representation leads to same results. We will discuss circuits with sine representation of A.C
    - Figure below shows the variation of A.C with time

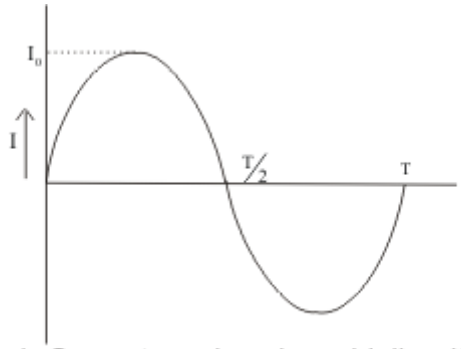


Figure 1. Current varying sinusoidally with time

- Complete set of variations of the current in one time period T is called cycle
- The emf or voltage whose magnitude changes sinusoidal with time is known as alternating emf and is represented by

$$V = V_0 \sin(\omega t + \phi) \qquad \text{----(3)}$$

where V_0 is the peak value of alternating current.

Average or mean current

- When an alternating current passed through a moving coil galvanometer it shows no deflection ,this is because for one complete cycle mean value of alternating current is zero as AC flows in one direction during one half cycle and in opposite direction during another half cycle.
- But mean value of A.C is finite over half cycle.
- So, mean or average value of AC is defined either for positive half cycle or for negative half cycle
- So,

$$i_{avg(T/2)} = \frac{\int_0^{T/2} i dt}{\int_0^{T/2} dt} = \frac{\int_0^{T/2} i_0 \sin(\omega t + \phi)}{\int_0^{T/2} dt} = \frac{2i_0}{\pi} \cong .636 i_0 \qquad \text{----(4)}$$

- From equation (4),we see that the average value of A.C during the half cycle is .636 times or 63.6% of its peak value
- Similarly we can show that

$$V_{avg(T/2)} = \frac{2V_0}{\pi} \cong .636 V_0$$

- During next half cycle mean value of ac will be equal in magnitude but opposite in direction.
- Always remember that mean value of AC over a complete cycle is zero and is defined over a half cycle of AC.

A.C through pure resistor

- Figure below shows the circuit containing alternating voltage source $V=V_0 \sin\omega$ connected to a resistor of resistance R

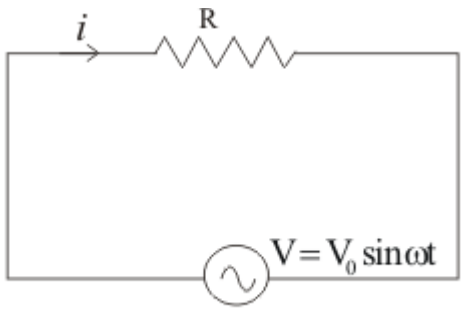


Figure 3. A.C. Circuit containing only resistor

- Let at any instant of time ,i is the current in the circuit ,then from Kirchhoffs loop rule

  $V_0 \sin\omega t - Ri$ (or)

  $i = (V_0/R)\sin\omega t$

  $= i_0 \sin\omega t$

  Where,

  $i_0 = V_0/R$
- From instantaneous values of alternating voltage and current ,we can conclude that in pure resistor ,the current is always in phase with applied voltage
- Their relationship is graphically represented as

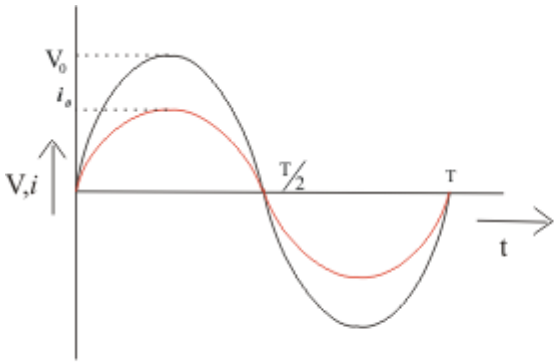


Figure 4(a). Sinusoidal representation

Figure 4(b). Phaser diagram representation of current and voltage through pure resistor

A.C through pure inductor

- Figure below shows the circuit in which voltage source

  $V = V_0 \sin\omega t$

  is applied to pure inductor (zero resistance) coil of inductance L

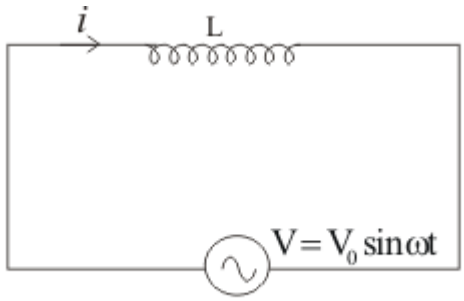


Figure 5. A.C. Circuit containing inductor of inductance L

- As the current through the inductor varies and opposing induced emf is generated in it and is given by -Ldi/dt
- From Kirchhoffs loop rule

$$V_0 \sin \omega t - L\frac{di}{dt} = 0$$

$$or,$$

$$di = \frac{V_0}{L} \sin \omega t \, dt$$

integrating on both the sides we get

$$i = -\frac{V_0}{\omega L} \cos \omega t + C$$

Where C is the constant of integration .This integration constant has dimensions of current and is independent of time. Since source has an emf which oscillates symmetrically about zero, the current it sustain also oscillates symmetrically about zero, so there is no time independent component of current that exists. Thus constant C=0

- So we have

$$i = \frac{-V_0}{\omega L} \cos \omega t$$

$$= \frac{V_0}{\omega L} \sin(\omega t - \frac{\pi}{2})$$

$$i = i_0 \sin(\omega t - \frac{\pi}{2})$$

where

$$i_0 = \frac{V_0}{\omega L}$$

is the peak value of current

- From instantaneous values of current and voltage (equation 11 and 10) we see that in pure inductive circuit the current lags behind emf by a phase angle of π/2

- This phase relationship is graphically shown below in the figure

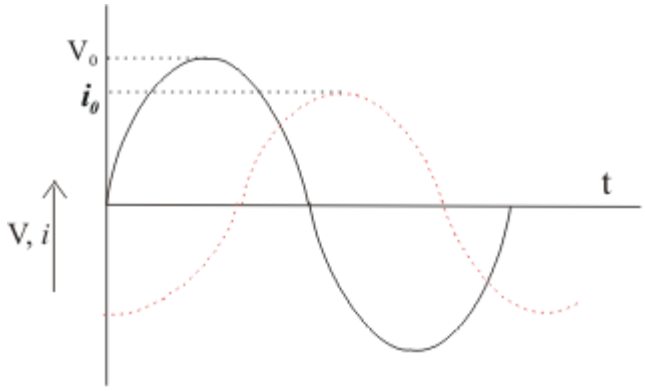


Figure 6 (a). Sinusoidal representation

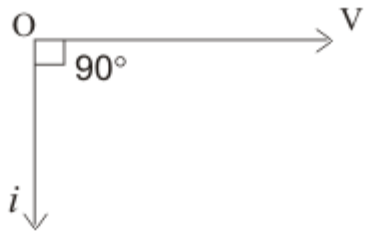


Figure 6 (b). Phaser diagram representation

- From above equation peak value of current in the coil is

$$i_0=V_0/\omega L$$

or

$$V_0=(\omega L)i_0$$

Comparing it with the ohm's law we find product ωL has dimension of resistance and it can be represented by

$$X_L=\omega L$$

where X_L is known as reactance of the coil which represents the effective opposition of the coil to the flow of alternating current

- $X_L=\omega L$ is zero for DC for which $\omega=0$ and increases as the frequency of current increases

AC through pure capacitor

- Figure given below shows circuit containing alternating voltage source $V=V_0\sin\omega t$ connected to a capacitor of capacitance C

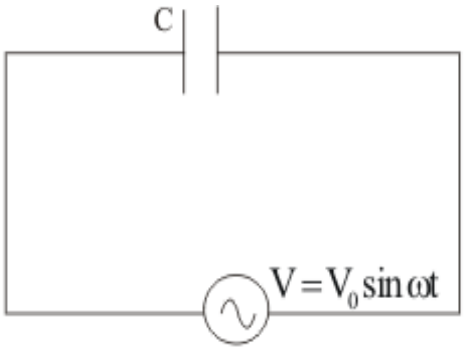


Figure 7. A.C. Circuit containing only capacitor

- Suppose at any time t,q be the charge on the capacitor and i be the current in the circuit
- Since there is no resistance in the circuit, so the instantaneous potential drop q/C across the capacitor must be equal to applied alternating voltage so $q/C=V_0\sin\omega t$

- Since i=dq/dt is the instantaneous current in the circuit so

$$i = \frac{dq}{dt} = \frac{d}{dt}(CV_0 \sin \omega t)$$

$$= CV_0 \omega \cos \omega t$$

$$= \frac{V_0}{(1/\omega C)} \cos \omega t$$

$$= i_0 \cos \omega t = i_0 \sin(\omega t + \frac{\pi}{2})$$

where

$$i_0 = \frac{V_0}{(1/\omega C)}$$

is the peak value of current

- Comparing equation with $V=V_0 \sin\omega t$,we see that in a perfect capacitor current leads emf by a phase angle of $\pi/2$
- This phase relationship is graphically shown below in the figure

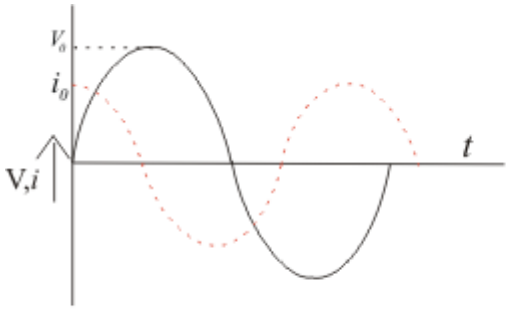


Figure 8 (a). Sinusoidal representation

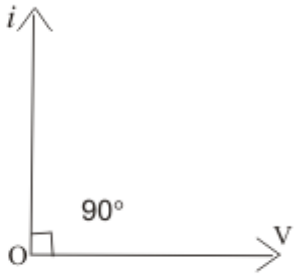


Figure 8 (b). Phaser diagram representation

- Again comparing peak value of current with ohm's law ,we find that quantity $1/\omega C$ has the dimension of the resistance
- Thus the quantity

$$X_C = 1/\omega C = 1/2\pi fC$$

is known as capacitive reactance

- From equation (14) we see that capacitive reactance decreases with increasing frequency of current and in infinite for direct current for which frequency f=0

Circuit containing inductance and resistance in series

- Figure below shows pure inductor of inductance L connected in series with a resistor of resistance R through sinusoidal voltage

$$V=V_0 \sin(\omega t+\varphi)$$

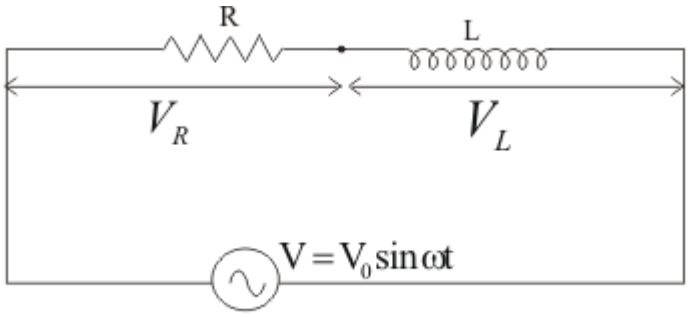


Figure 9. A.C. Circuit containing inductor and an resistor

- An alternating current I flowing in the circuit gives rise to voltage drop V_R across the resistor and voltage drop V_L across the coil
- Voltage drop V_R across R would be in phase with current but voltage drop across the inductor will lead the current by a phase factor $\pi/2$
- Now voltage drop across the resistor R is

  $V_R=IR$

  and across inductor

  $V_L=I(\omega L)$

  where I is the value of current in the circuit at a given instant of time
- So voltage phasors diagram is

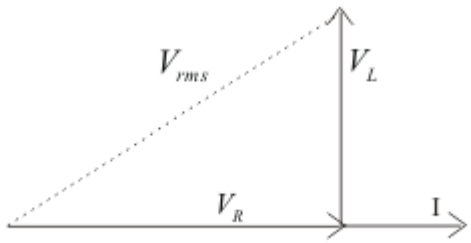


Figure 10. Voltage phasor diagram for LR series circuit

In figure (10) we have taken current as a reference quantity because same amount of current flows through both the components. Thus fro phasors diagram

$$V = \sqrt{V_R^2 + V_L^2}$$
$$= I\sqrt{R^2 + \omega^2 L^2}$$
$$= IZ$$

where

$$Z = \left(R^2 + \omega^2 L^2\right)^{1/2}$$

is known as impedance of the circuit

- Current in steady state is

$$I = \frac{V_0 \sin(\omega t - \phi)}{Z}$$

and it lags behind applied voltage by an angle φ such that $\tan\varphi=\omega L/R$

Circuit containing capacitance and resistance in series

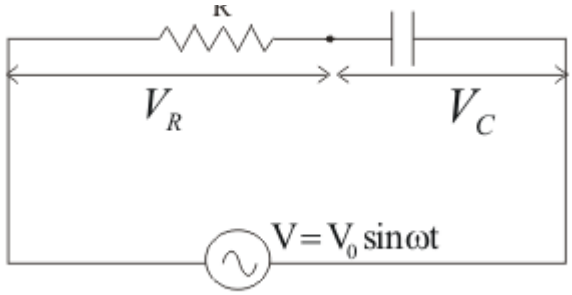


Figure 11(a). A.C. Circuit containing capacitor and an resistor

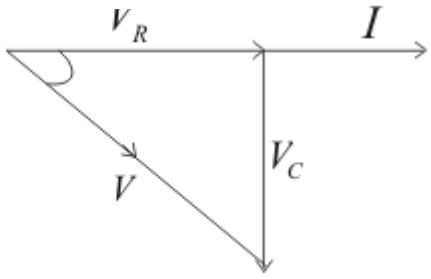


Figure 11(b). Phasor digram

- Figure below shows a circuit containing capacitor and resistor connected in series through a sinusoidal voltage source of voltage
  $V=V_0\sin(\omega t+\varphi)$

- In this case instantaneous P.D across R is
  $V_R=IR$
  and across the capacitor C is
  $V_C=I/\omega C$
- In this case V_R is in phase with current i and V_C lags behind i by a phase angle 90_0
- Figure 11(b) shows the phasors diagram where vector OA represent the resultant of V_R and $V_C$which is the applied Voltage thus

$$V = \sqrt{V_R^2 + V_C^2}$$
$$= i\sqrt{R^2 + \frac{1}{\omega^2 C^2}}$$
$$= iZ$$

where

$$Z = \sqrt{R^2 + \frac{1}{\omega^2 C^2}}$$

is called the impedance of the circuit

- Again from the phasors diagram applied voltage lags behind the current by a phase angle φ given by $\tan\varphi= V_C/ V_R=1/\omega CR$

LCR series circuit

- Figure below shows a circuit containing a capacitor ,resistor and inductor connected in series through an alternating voltage source

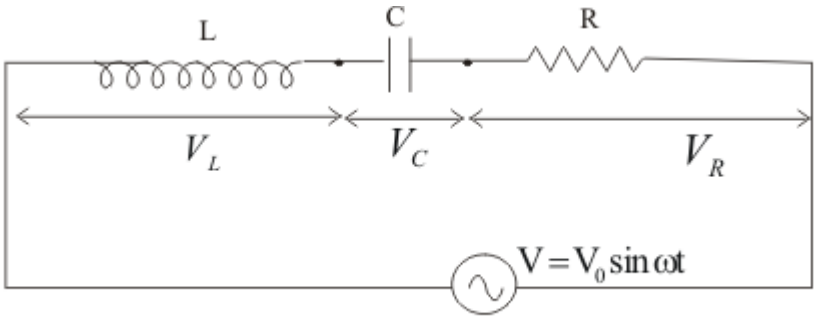


Figure 12(a). A.C. Circuit containing inductor capacitor and an resistor in series

- Same amount of current will flow in all the three circuit components and vector sum of potential drop across each component would be equal to the applied voltage
- If i be the amount of current in the circuit at any time and V_L,V_C and V_R the potential drop across L,C and R respectively then

  $V_R = iR \Rightarrow$ Voltage is in phase with i

  $V_L = i\omega L \Rightarrow$ Voltage is leading i by 90^0

  $V_C = i/\omega C \Rightarrow$ Voltage is lagging behind i by 90^0
- Since V_L is ahead of i by 90 and V_C is behind by 90 so that phase difference between V_L and V_C is 180 and they are in direct opposition to each other as shown in the figure 12(b)

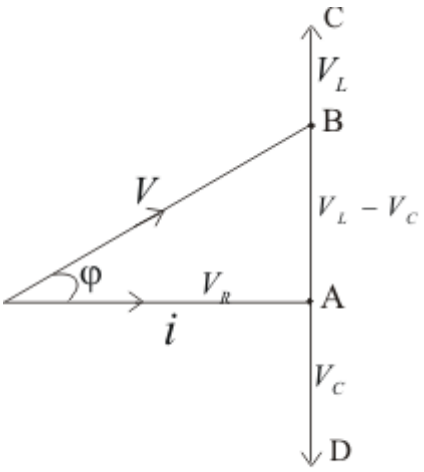


Figure 12(b). Phasor diagram

- In figure 12(b) we have assumed that V_L is greater than V_C which makes i lags behind V.If $V_C > V_L$then i lead V
- In this phasors diagram OA represent V_R,AD represent V_C and AC represent V_L.So in this case as we have assumed that $V_L > V_C$,there resultant will be $(V_L - V_C)$ represented by vector AD
- Vector OB represent resultant of vectors V_R and $(V_L - V_C)$ and this vector OB is the resultant of all the three ,which is equal to applied voltage V,thus

$$V = \sqrt{V_R^2 + (V_L - V_C)^2}$$
$$= i\sqrt{R^2 + (X_L - X_C)^2}$$
$$= i\sqrt{R^2 + (\omega L - \frac{1}{\omega C})^2}$$
$$= iZ$$

where

$$Z = \sqrt{R^2 + (\omega L - \frac{1}{\omega C})^2}$$

is called impedance of the circuit

- From phasors diagram 12(b),current i lag behind resultant voltage V by an phase angle given by,

$$\tan\phi = \frac{V_L - V_C}{V_R} = \frac{X_L - X_C}{R} = \frac{\omega L - \frac{1}{\omega C}}{R}$$

- From equation (20) three cases arises
  (i) When ωL > 1/ωC then tanφ is positive i.e. φ is positive and voltage leads the current i
  (ii) When ωL < 1/ωC,then tanφ is negative i.e. φ is negative and voltage lags behind the current i
  (iii) When ωL = 1/ωC ,then tanφ is zero i.e. φ is zero and voltage and current are in phase
- Again considering case (iii) where ωL = 1/ωC,we have

$$Z = \sqrt{R^2 + (\omega L - \frac{1}{\omega C})^2} = R$$

- which is the minimum value Z can have.

- This is the case where X_L=X_C,the circuit is said to be in electric resonance where the impedance is purely resistive and minimum and currents has its maximum value

- Hence at resonance
  ωL = 1/ωC or ω=1/√LC
  But ω=2πf where f is the frequency of applied voltage .Therefore f_0=1/2π√LC

  This frequency is called resonant frequency of the circuit and peak current in this case is i_0=V_0/R and reactance is zero

- We will now define resonance curves which shows the variation in circuit current (peak current i_0) with change in frequency of the applied voltage

- Figure below shows the shape of resonance curve for various values of resistance R

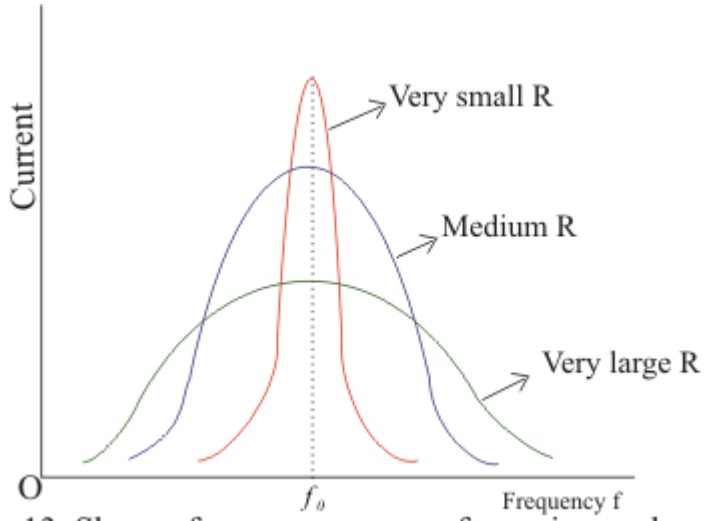


Figure 13. Shape of resonance curves for various values of R

- for small value of R,the resonance is sharp which means that if applied frequency is lesser to resonant frequency f_0,the current is high otherwise

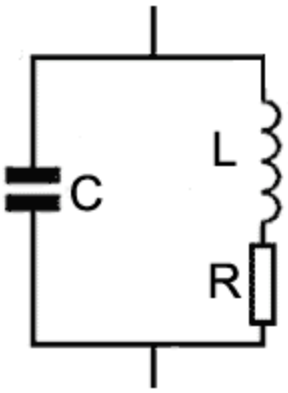
- For large values of R,the curve is broad sided which means that those is limited change in current for resonance and non -resonance conditions

The LCR Parallel Resonant Circuit

- In many ways a parallel resonance circuit is exactly the same as the series resonance circuit we looked at in the previous tutorial.

- Both are 3-element networks that contain two reactive components making them a second-order circuit, both are influenced by variations in the supply frequency and both have a frequency point where their two reactive components cancel each other out influencing the characteristics of the circuit.

- Both circuits have a resonant frequency point. The difference this time however, is that a parallel resonance circuit is influenced by the currents flowing through each parallel branch within the parallel LC tank circuit. A tank circuit is a parallel combination of L and C that is used in filter networks to either select or reject AC frequencies. Consider the parallel RLC circuit below



LCR Parallel Circuit

Let us define what we already know about parallel RLC circuits.

Admittance $y = 1/Z = \sqrt{G^2-B^2}$

Conductance $G = 1/R$

Inductive Suceptance $B_L = 1/2\pi fL$

Capacitive sucspectance $Bc = 2\pi fC$

- A parallel circuit containing a resistance, R, an inductance, L and a capacitance, C will produce parallel resonance (also called anti-resonance) circuit when the resultant current through the parallel combination is in phase with the supply voltage.
- At resonance there will be a large circulating current between the inductor and the capacitor due to the energy of the oscillations, then parallel circuits produce current resonance.
- A parallel resonant circuit stores the circuit energy in the magnetic field of the inductor and the electric field of the capacitor.
- This energy is constantly being transferred back and forth between the inductor and the capacitor which results in zero current and energy being drawn from the supply.
- This is because the corresponding instantaneous values of I_L and I_C will always be equal and opposite and therefore the current drawn from the supply is the vector addition of these two currents and the current flowing in I_R.
- In the solution of AC parallel resonance circuits we know that the supply voltage is common for all branches, so this can be taken as our reference vector.

- Each parallel branch must be treated separately as with series circuits so that the total supply current taken by the parallel circuit is the vector addition of the individual branch currents.
- Then there are two methods available to us in the analysis of parallel resonance circuits. We can calculate the current in each branch and then add together or calculate the admittance of each branch to find the total current.
- We know from the previous series resonance tutorial that resonance takes place when $V_L = -V_C$ and this situation occurs when the two reactance are equal, $X_L = X_C$. The admittance of a parallel circuit is given as:

$$Y=G+B_L+B_C$$

$$Y= 1/R+ 1/j\omega L+j\omega C \text{ (or)}$$

$$Y= 1/R + 1/2\pi fL +2\pi fC$$

Resonance occurs when $X_L = X_C$ and the imaginary parts of Y become zero. Then:

$$X_L= X_C$$

$$2\pi fL = 1/2\pi fC$$

$$f^2 - 1/(2\pi L \times 2\pi C) = 1/4\pi^2 LC$$

$$f = \sqrt{1/4\pi^2 LC}$$

$$f_r = 1/(2\pi\sqrt{LC}) \text{ (or)}$$

$$\omega_r = 1/\sqrt{LC}$$

- Notice that at resonance the parallel circuit produces the same equation as for the series resonance circuit. Therefore, it makes no difference if the inductor or capacitor is connected in parallel or series.
- Also at resonance the parallel LC tank circuit acts like an open circuit with the circuit current being determined by the resistor, R only. So the total impedance of a parallel resonance circuit at resonance becomes just the value of the resistance in the circuit and Z = R as shown.
- **Q-factor**: In LCR Circuit, the ratio of resonance frequency to the difference of its neighbouring frequencies so that their corresponding current is 1/2 times of the peak value, is called Q-factor of the circuit.

  Formula: $Q=1/R\sqrt{L/C}$

  Conditions for the large value of Q factor:
  (i) Value of L/C should be large.
  (ii) Value of R should be less.

APPLIED PHYSICS-I

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SOURCE:

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