KUNTHAVAI NAACHIYAR GOVT. ARTS COLLEGE FOR WOMEN (A)
THANJAVUR -7.

DEPARTMENT OF PHYSICS

M.SC., PHYSICS STUDY MATERIAL

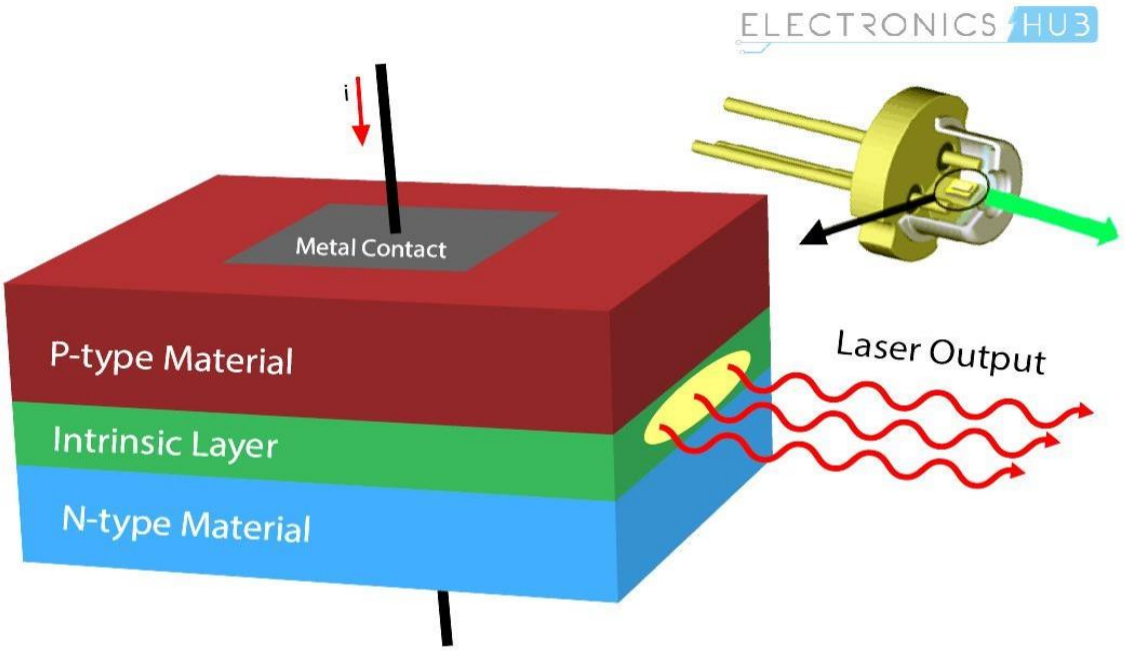
SUB. CODE: 18KP1PELP1

SUB TITLE: ANALOG AND DIGITAL ELECTRONICS

UNIT 1

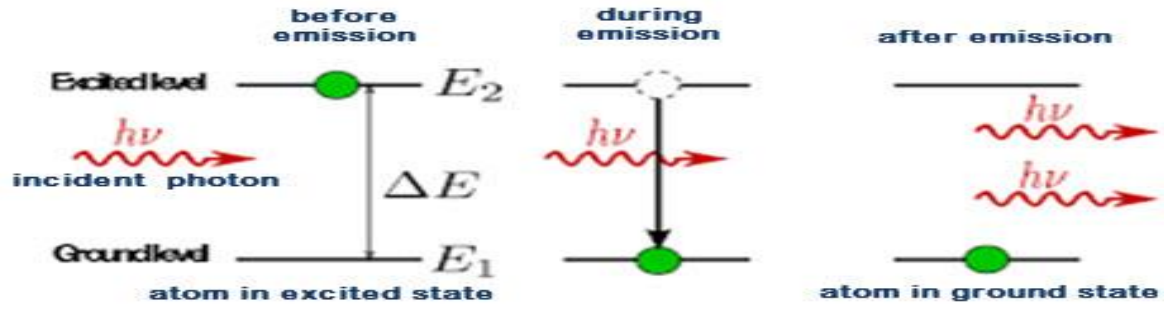
Semiconductor LASER Diodes

A heavily doped P- region is produced by diffusion of Zn into N-type Ga As. The doping in the N and P regions is such that both are degenerate. The depletion layer whose thickness is usually very small (0.1 micro meter). To obtain laser action, one pair of faces, perpendicular to junction plane is cleaved and polished so that they act as reflecting mirrors. The remaining two faces are left unfinished to suppress the lasing in these directions. In this way the structure acts as resonant cavity and is called Fabry-Perot cavity.



LASER DIODE CONSTRUCTION

Operation: As the material iis heavily doped, the Fermi level of P-type falls within the valence band while that of N-type falls within the conduction band. When no voltage is applied, the two Fermi levels lie in the same horizontal line. The two bands are separated by an energy gap E_g known as forbidden band. Due to this gap, conduction electrons cannot occupy the holes in N-type material.



$$E_2 - E_1 = \Delta E = h\nu$$

Now consider P_N junction is forward biased with an external voltage V such that ev > E_g . Now electrons are attracted towards P region and holes towards N region. They overlap atleast in a small region near the junction known as depletion region. In depletion region the injected electrons and holes both appear in high concentration. A high hole concentration means a large number of empty state into which electrons can fall. Thus population inversion is achieved. Laser action follows in this region. Initially, at low current, there is spontaneous emission in all directions. As the bias is increased, eventually a thereshold current is reached at which the stimulated emission occurs. Thus a monochromatic and highly directional beam of light is emitted from the junction.

Laser diodes have been fabricated with emission wavelengths extending from the visible to infrared region using various semiconductors.

Applications of Laser Diode

i)Low power Lasers are used in an increasing number of familiar applications including CD and DVD players and recorders, bar code readers, security systems, optical communications and surgical instruments.

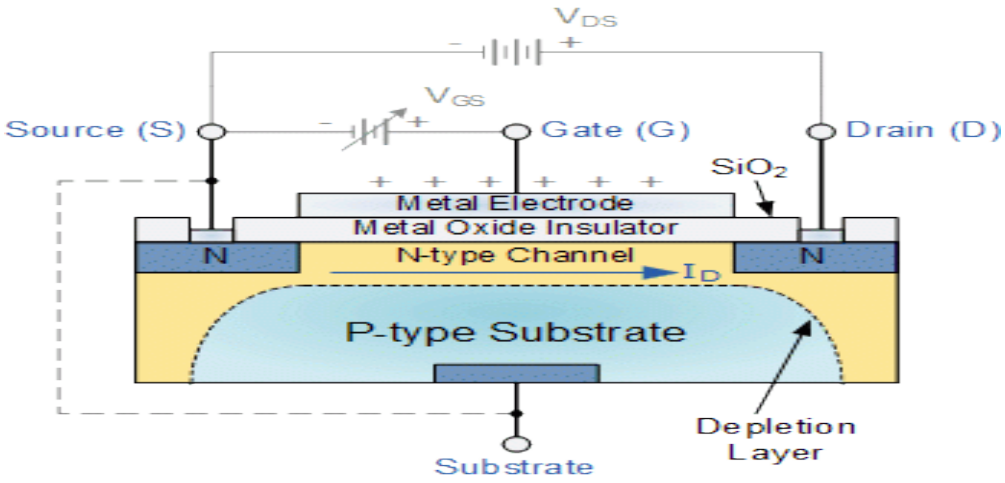
ii)Engraving, cutting, scribing, drilling, welding, etc. Medical applications remove unwanted tissues, diagnostics of cancer cells using fluorescence, dental medication. In general, the results using lasers are better than the results using a surgical knife.

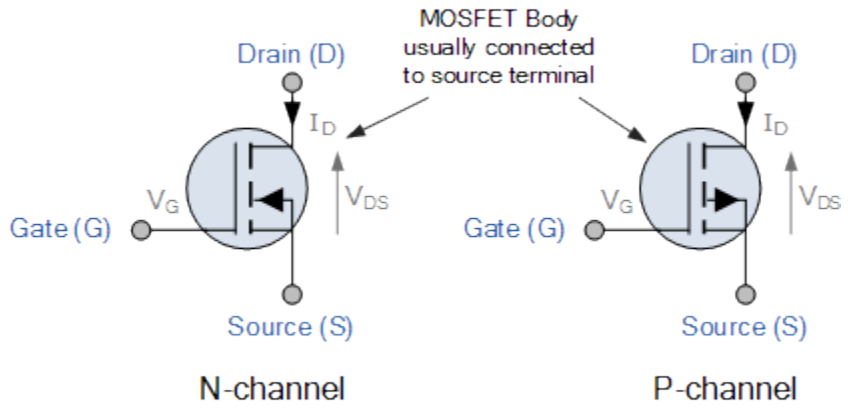
iii) In the telecom field 1.3 μm and 1.55 μm band laser diodes used as the main light source for silica fibre lasers have a less transmission loss in the band. The laser diode with the different band is used for pumping source for optical amplification or for the short-distance optical link.

METAL OXIDE SEMICONDUCTOR FET (MOSFET)

There two type of metal oxide semiconductor FET. The first type is know as enhancement type MOSFET, while the second type as depletion MOSFET.

Enhancement type (MOSFET) : An N channel MOSFET is shown in fig . There are two highly doped (N+) regions (one source and the other drain) on a lightly doped P type(substrate). A layer of insulating silicon di-oxide is place over it . Now over the insulating Sio_2 layer a gate is formed. Three different terminals for source, gate and drain are taken out as shown in figure . The insulating layer between gate and channels provides a very high input impedance.

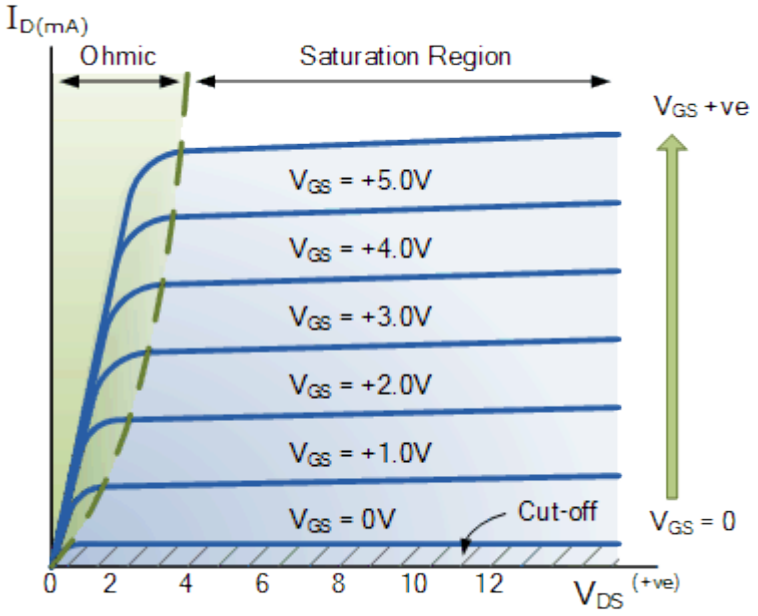




.

In order to consider the operation of this MOSEFT , let us consider thet $V_{GS} = 0$. Let a positive voltage is appied between drain and source ($_{VDS}$) as shown. As there is no channel and hence the drain current is zero . Now consider that V_{GS} is increased . The positive potential at gate terminal will repel the holes present in P-type substrate. As a result, the concentration of electrons near Sio_2 layer inside substrate increases . The further increase in V_{GS} increases the number of electrons near Sio_2 layer as shown in the figure . After further increases in the value of V_{GS} , the electron concentration increases to such an extent that it creates an induced N- channel. Now drain current start flowing through this channel. The value of V_{GS} at which the drain current stats flowing is called as threshold voltage and is denoted by V_T .

Fig . shown the drain charateristis and transfer characteristics of N- channel enhancement type MOSEFT .



It may be noted from fig that the drain current for V_{GS} greater than zero is very small and as V_{GS} is made positive the current increases slowly at first and then at a much more rapid rate . The gate source voltage at which the channel is formed to let through the flow of drain current of predefined value (say 10 μA) is called the gate source threshold value. The gate source

threshold value ia denoted by V_{GST} or simply V_T as shown in fig . The current $I_{D\,(on)}$ represents the maximum permissible current on the drain characteristics. These value (V_{GST} and $I_{D\,(ON)}$) are sometimes specified by the manufacturer for particular MOSEFT .

DEPLETION MOSEFT : fig. shown the construction of N-channel depletion type MOSEFT. It consists of a lightly doped P-type semiconductor bar (silicon) which works as substrate . Into the substrate , two highly doped N-regions are diffused . These regions are called as source and drain . A thin layer of insulating silicon dioxide (Sio_2) is grown over the surface of substrate . Two holes are cut into insulating layer for allowing the metallic contacts with source and drain for electrical connections . The third terminal is gate as shown in figure . The different between depletion MOSEFT and enhancement MOSEFT is that in depletion MOSEFT an N-type channel is also introduction between source and drain . It is important to mention here that there is a no contact between gate terminal and N-type channel, i.e, the gate terminal insulated from N-type channel by Sio_2 layer . Due to N-type channel, there will be an appreciable drain current I_{DSS} for $V_{GS} = 0$ V.

Due to the presence of SiO_2 layer between gate and N-channel, the input impedance of this MOSEFT is very high .

Operation : Let us consider the case when $V_{GS}= 0$ and a positive voltage is applied between drain and source . In this situation, gate, source and substrate terminals are connected to ground as shown in fig. As positive voltage is applied at drain terminal , the free electron from N-channel are attracted towards drain terminal . This cause the current to flow through the channel as shown in the figure . The current is denoted as I_{DSS} at $V_{GS} = 0$ V.

Let us consider the effect of negative gate voltage (- V_{GS}). Fig shown the effect of negative gate to source voltage on drain current . The negative voltage on gate will repel the electron towards P-type substrate and attract the hole from substrate (where they are in majority). There will be recombination of repelled electrons and attracted holes as shown in the figure . As a result, the number of conduction electron in the channel reduces. Consequently, the drain current decreases. As the negative voltage on gate is further reduced, there will be a greater reduction in conduction electron, i.e., further decreases in drain current.

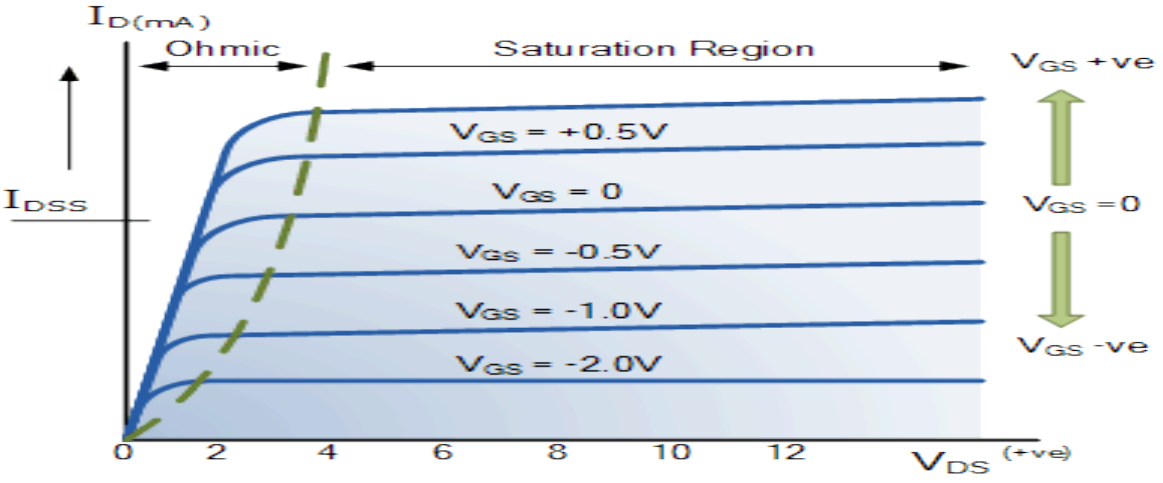


Fig shown the drain characteristic and transfer characteristic for an N-channel MOSEFT which can be operated in both depletion mode and enhancement mode MOSEFT may be designated a dual mode MOSEFT.

Let us now consider the effect of positive gate to source voltage. Due to positive voltage , the gate attracts more electrons from P-type substrate where they are present as minority carriers. These accelerated electrons will knock at more electrons due to collision. So, positive gate to source voltage increases the drain current . The rise in drain current with increases V_{GS} will be very rapid . We should be aware of the maximum drain current rating.

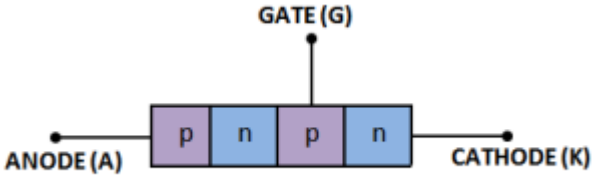
Thus , the positive gate voltage 'enchances' the level of conduction electrons in the channel while the negative gate voltage reduces 'deplete off ' the number of conduction electron in the channel . Due to this reason , the MOSEFT working with negative gate voltage is called to be working with depletion mode and MOSEFT with positive gate voltage is called to be working in enhancement mode.

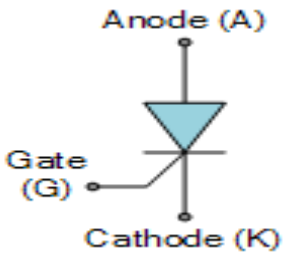
It is obvious from fig, that for V_{GS}= 0, the drain current is not zero but has appreciable value. The figure shows the gate source cut off voltage $V_{GS(off)}$ at which the drain current I_D reduces to some specified negligible value at a recommended drain voltage V_{DS}. This voltage $V_{GS(off)}$ corresponds to a pinch off voltage V_P of a JFET . The operation and the characteristics of a P-channel MOSEFT are similar to N-channel MOSEFT except that the signs of currents and voltage are reversed .

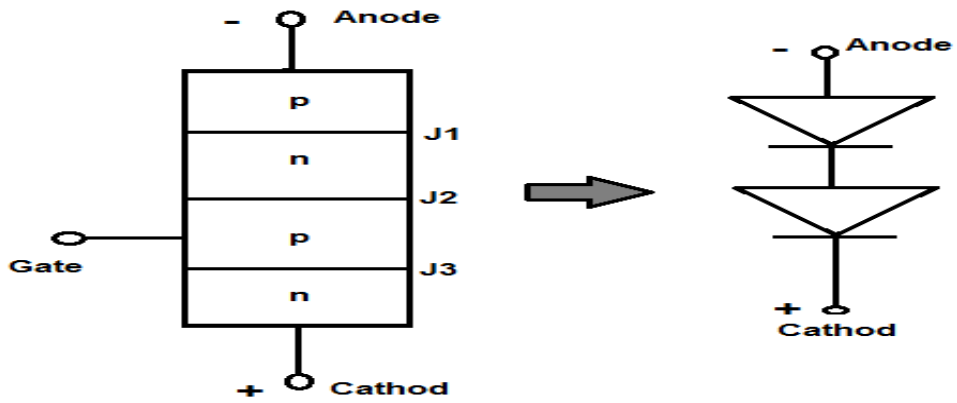
CHARACTERISTICS OF SCR

The SCR has appeared in the market under different names such as thyristor, thyrode transistor. Like the diode, SCR is a unidirectional device,i.e. it will only conduct current in one direction only, but unlike a diode, the SCR can be made to operate as either an open-circuit switch or as a rectifying diode depending upon how its gate is triggered.

In other words, SCR can operate only in the switching mode and cannot be used for amplification. Hence, it is extensively used in switching d.c. and a.c., rectifying a.c. to give controlled output, converting d.c. into a.c. etc.







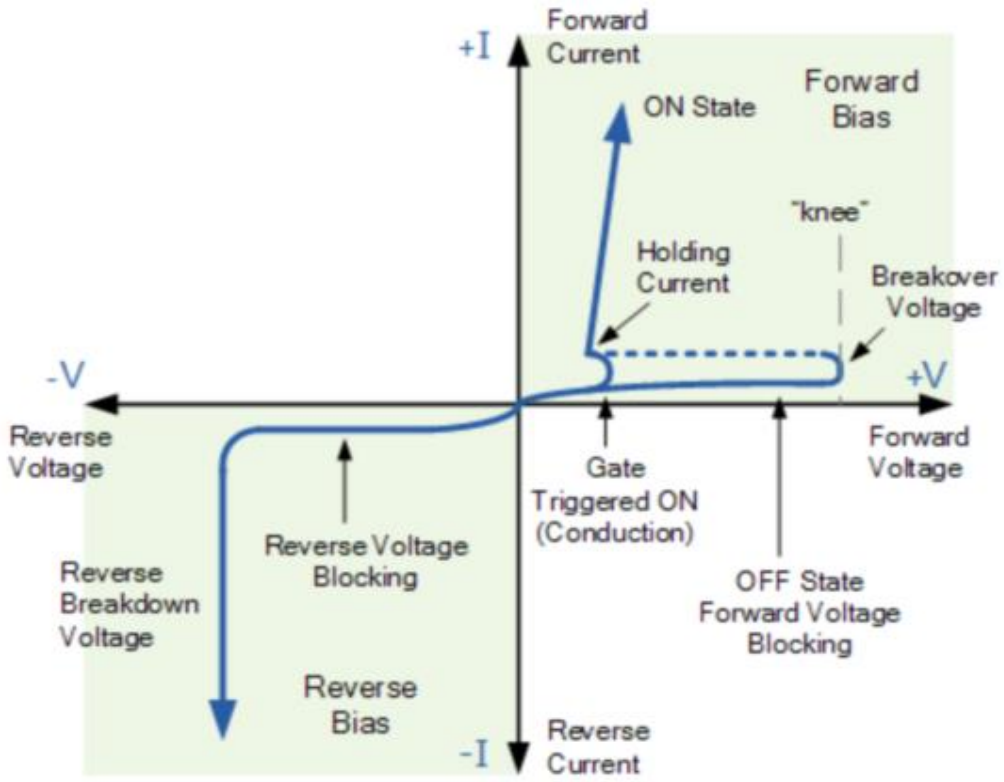
This is a four layer PNPN device. It consists of three junctions J_1, J_2, J_3 (J_1, and J_3 operate in forward direction while middle J_2 operates in reverse direction). Three terminals are taken; one from the outer p-type material called anode A, second from the outer layer of n-type material called cathode K and the third from the base of transistor section and is called gate G.

Let the SCR is cut along the dotted line as shown in fig. Now we have two devices as shown in fig. The upper part is a PNP transistor while the lower part is NPN transistor, the base of PNP transistor is connected to the collector of NPN transistor while the collector of PNP transistor is connected to the base of NPN transistor. The gate terminal is taken out from the base of NPN transistor.

OPERATION OF SCR

The equivalent circuit of SCR with supply voltage v applied between anode and cathode with a load resistor R_L is shown in fig. When the gate is open, i.e., switch S is open, the SCR is in OFF state. Let a trigger pulse is applied at the gate or a voltage is applied by closing switch S, the SCR is in ON state. The reason is as follows: By applying triggering pulse or voltage to the gate, a gate current flows through the base of T_2. This increases the collector current of T_2.

As it is obvious from the figure that the collector current of T_2 is the base current of T_1 and hence the collector current of T_1 increases. This forms the input base current to T_2 which undergoes further amplification by T_2. In this way, both transistors feedback each other. The process is very quick and soon both the transistors are driven to saturation. The current through the ON state of SCR is controlled by external resistance R. Once the device is in ON state, the gate loses its control and the device remains in conducting state even if the gate is opened.

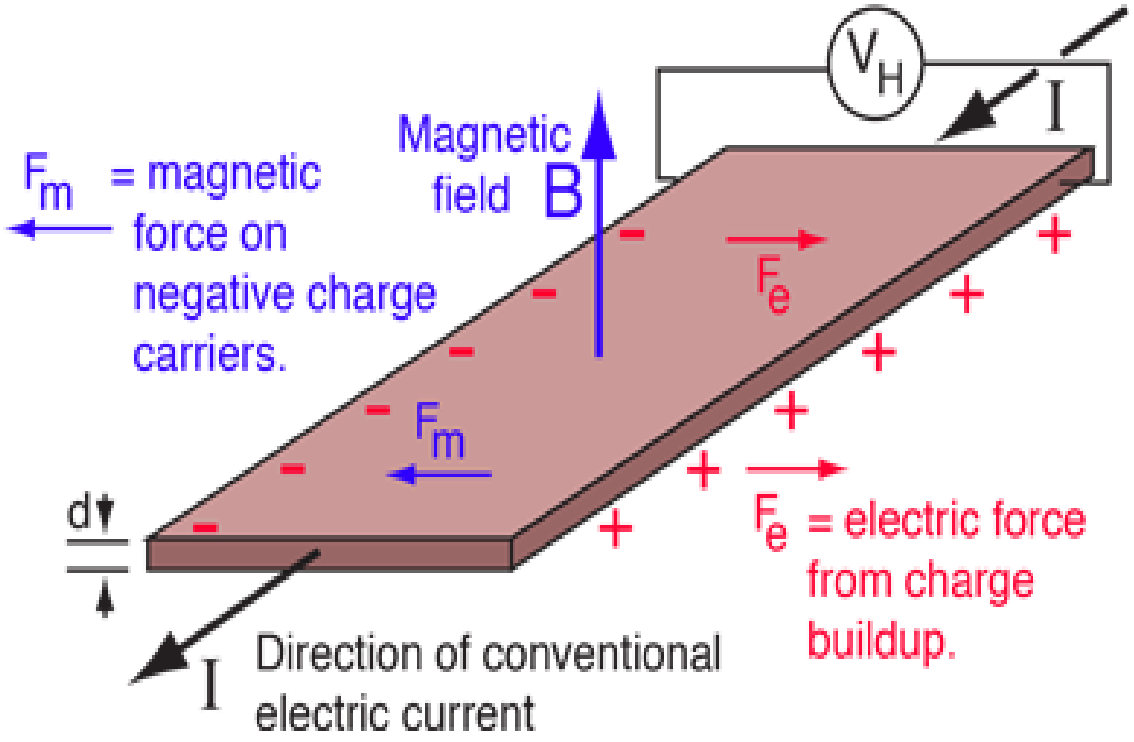


Let us consider the case of forward bias. In this case too, a small leakage current follows. This current flows due to thermally generated minority carrier. The solid curve on right hand side shows the leakage current for no gate current. When forward voltage is increased, a breakdown condition is reached which fires SCR. The voltage at which SCR fires is called as forward break over voltage. This is denoted by V_{BO} . if a positive gate current is supplied, the SCR can become conducting at a voltage much lesser than forward breakdown voltage as indicated by dotted curve for I_{G1} . The larger is the gate current, lower is the breakdown voltage. Once the SCR is switched ON, the forward voltage drop across it is suddenly reduced to a very small value.

If the forward voltage is less than the forward break over voltage V_{BR} , the firing of SCR can also be made by applying a short positive pulse current at the gate. The method is called as gate control. This is denoted by line OB, SCR remains conducting as long as the anode current is maintained larger than holding current I_H . If anode current becomes less I_H, SCR Off. It is important to mention here that the gate can only switch ON the SCR but it cannot switch OFF.

HALL EFFECT

When a magnetic field is applied perpendicular to a current carrying conductor, a voltage is developed across the specimen in a direction perpendicular to both the current and the magnetic field. This iphenomenon is called the ‘Hall effect”. The voltage so developed is called the ‘Hall voltage’**.**



If an electric current flows through a conductor in a magnetic field, the magnetic field exerts a transverse force on the moving charge carriers which tends to push them to one side of the conductor. This is most evident in a thin flat conductor as illustrated. A build up of charge at the sides of the conductors will balance this magnetic influence, producing a measurable voltage between the two sides of the conductor. The presence of this measurable transverse voltage is called the Hall effect after E. H. Hall who discovered it in 1879.

Note that the direction of the current I in the diagram is that of conventional current, so that the motion of electrons is in the opposite direction. That further confuses all the "right-hand rule" manipulations you have to go through to get the direction of the forces.

The electric force on the electron having a charge $e = -eE_x$

The force due to the magnetic field $= ev_x H_z$.

In the steady state $F_y = 0$.

$$F_y = -eE_y + e(v_x H_z) = 0$$

or $$E_y = v_x H_z$$

E_y is called the *Hall voltage* or *Hall field*.

Let n be the free electron density.

The current density is given by

$$J_x = -nev_x$$

$$v_x = -\frac{J_x}{ne}$$

$\therefore$ $$E_y = v_x H_z = -\frac{J_x H_z}{ne} = R_H J_x H_z$$

Here, $R_H = -\frac{1}{ne}$ is called the '*Hall coefficient*' for the substance of the bar.

The negative value of R_H indicates that current carriers are electrons. If the charge carriers are holes, R_H is positive.

Relation between R_H and μ

The mobility 'μ' is defined as the velocity acquired by the current carrying particle per unit electric field, *i.e.*,

$$\mu = \frac{v_x}{E_x} \quad \therefore v_x = \mu E_x$$

Eq. (3) becomes $$E_y = \mu E_x H_z$$

Comparing Eqs. (3) and (4),

$$R_H J_x H_z = \mu E_x H_z$$

$$R_H = \mu \frac{E_x}{J_x}$$

$\therefore$ $$R_H = \mu \cdot \frac{1}{\sigma}$$

Here, σ is the electrical conductivity of the metal.

$\therefore$ $$\mu = R_H \sigma.$$

57.2 Experimental Determination of Hall Coefficient

A thin metallic strip, several mm wide and several cm long, is placed in x-direction and a magnetic field H_z is applied in z-direction (Fig. 57.2).

A suitable current is passed in the specimen which can be adjusted by the rheostat. Two potential leads are placed between the points A and B

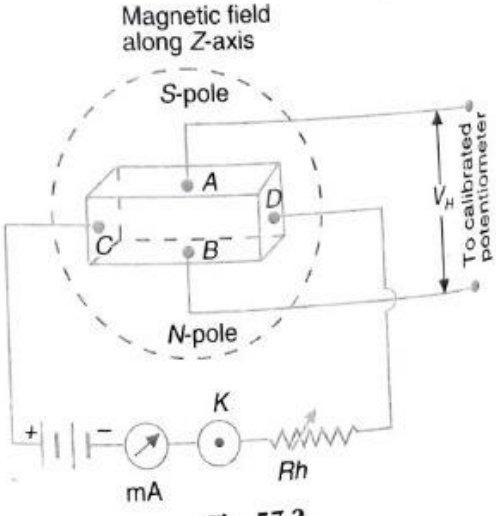
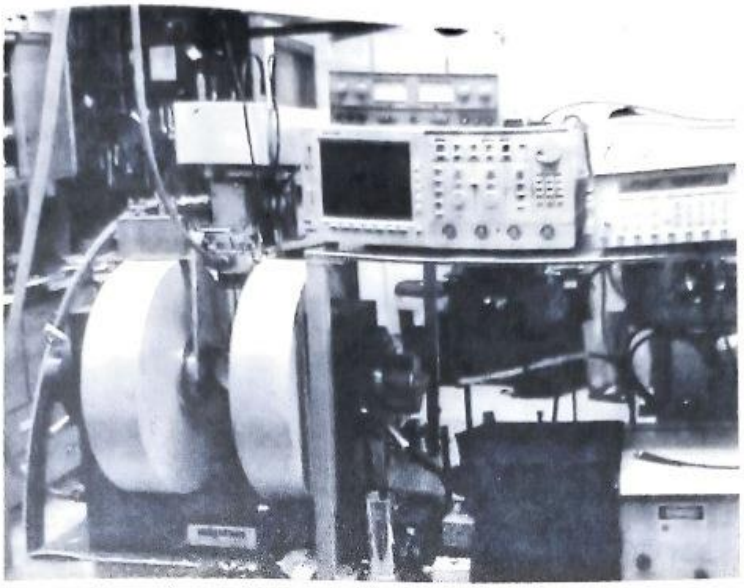


Fig. 57.2



Experimental Determination of Hall Coefficient.

which are connected to a sensitive calibrated potentiometer to measure the developed Hall voltage V_H. By measuring the Hall voltage, Hall-coefficient can be calculated as given below :

The value of Hall electric field is given by

$$E_y = -\frac{J_x H_z}{ne}$$

Let I be the current flowing through the specimen.

Let b and d be respectively the breadth and thickness of the specimen.

The current density is given by

$$J_x = \frac{I}{b \times d}$$

$$E_y = -\frac{I}{nebd} \cdot H_z$$

or
$$E_y \cdot d = V_H = -\frac{1}{neb} \cdot H_z = R_H \cdot \frac{I H_z}{b}$$

Hall coefficient,
$$R_H = \frac{V_H \cdot b}{I H_z}.$$

Thus, the value of Hall coefficient (R_H) can be calculated by knowing I and H_z and by measuring experimentally the Hall voltage V_H developed across the points A and B by means of a calibrated potentiometer.

Applications. The Hall effect measurements provide the following information about the solid:

1. The sign (electrons or holes) of charge carrier is determined.
2. The carrier concentration (number of charge carriers per unit volume) is determined.
3. The mobility of charge carriers is measured directly.
4. We can decide whether a material is a metal, semiconductor or insulator.
5. From the knowledge of measured Hall voltage, the unknown magnetic field can be measured provided the value of Hall constant for the slab is known.

UNIJUNCTION TANNSISTOR (UJT)

A Uni Junction Transistor (abbreviated as UJT) is a three terminal semiconductor switching device. It is used in switching circuits requiring rapid discharge of a capacitor fig. (88a) shows the structure of UJT shows the symbolic representation. It consist of a lightly doped N- type silicon bar with a heavily doped P type material alloyed to its one side . for producing single P-N junction. At the ends of silicon bar electrical connections are made . The leads at these connection are called as base 1(B_1) and base 2 (B_2) . The terminal brought out from P-type material is called emitter (E) . In the symbolic representation , the arrow in the emitter points in the direction of forward current through the junction and inclined towards B_1 terminal. Following points should be remembered in case of UJT:

i. It has one P-N junction .
ii. It differs from an ordinary diode that it has three leads .
iii. It differs from a FET that its emitter junction is much smaller than the gate surface of a FET.
iv. UJT is operated with emitter junction forward –biased while FET is usually operated with the gate junction as reverse-biased .
v. It has no ability to amplify while it has ability to control a large a.c. power with small signal .
vi. It exhibits a negative resistance characteristic and hence it can be used as an oscillator .

Inter base resistance (R_{BB}) : The total resistance of the silicon bar , i.e., the resistance between $B_1$and B_2 with emitter terminal open is called as inter base resistance . It is of the order of 5 + 10 kΩ . The inter base resistance is represented by two resistors in series.

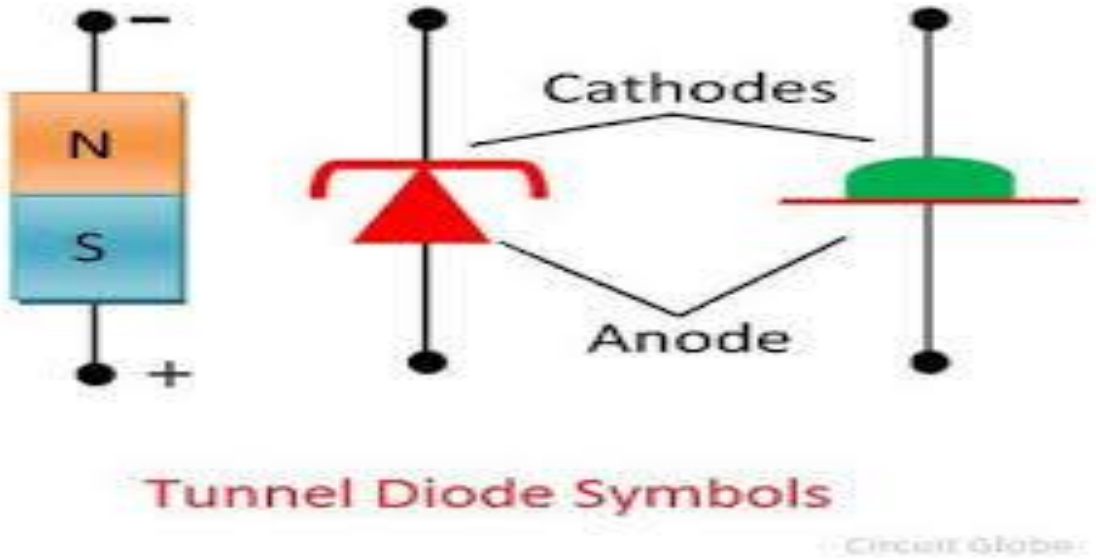
$$R_{BB} = R_{B2} + R_{B1} ,$$

Where R_{B2} is the resistance of silicon bar between B_2 and the points at which emitter junction lies and R_{B1} is the resistance of silicon bar between B_1 and emitter junction . The resistance R_{B1} is variable because its value depends upon the bias voltage across P-N junction . Usually $R_{B1} > R_{B2}$ and R_{B1} = 60% of R_{BB} .

Intrinsic stand – off ratio : Fig .(89) shows a battery V_{BB} connected across B_2 B_1 of equivalent circuit of UJT . Here emitter point E acts as a voltage divider tap on the fixed resistance R_{BB} . It is obvious that part of V is dropped over R_{B2} and part on R_{B1} Let the voltage drop across R_{B1} is V_A . According to simple voltage divider rule .

TUNNEL DIODE

A **tunnel diode** (also known as a **Esaki diode**) is a type of semiconductor diode that has effectively "negative resistance" due to the quantum mechanical effect is called tunneling. Tunnel diodes have a heavily doped PN junction that is about 10 nm wide. The heavy doping results in a broken band gap, where conduction band electron states on the N-side are more or less aligned with valence band hole states on the P-side.

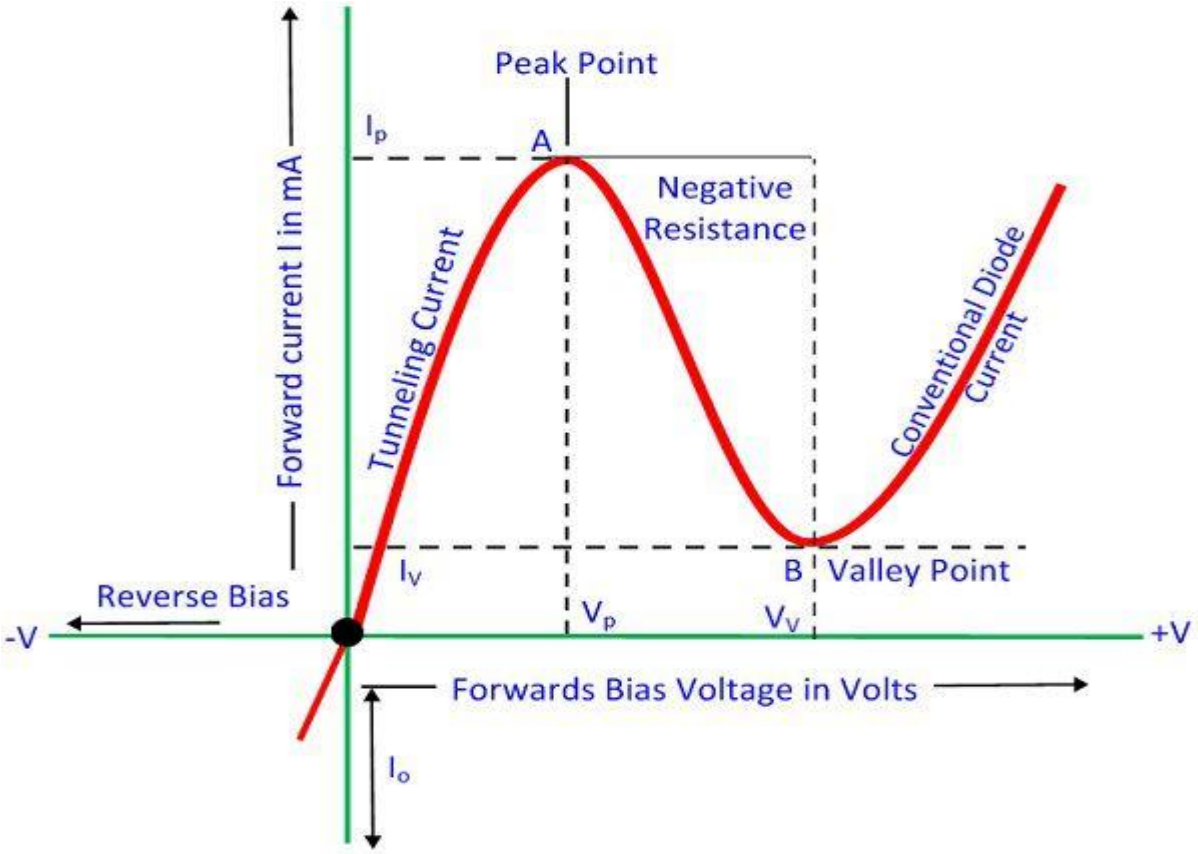


A mechanism of conduction in which charge carriers having a very little energy punch through the barrier directly instead of climbing over it is called tunnelling. Due to this reason the diode is known as tunnel diod.

A tunnel diode is a high conductivity two terminal p-n junction diode doped heavily about 1000 times higher than a conventional junction diode.

Volt-Ampere characteristic

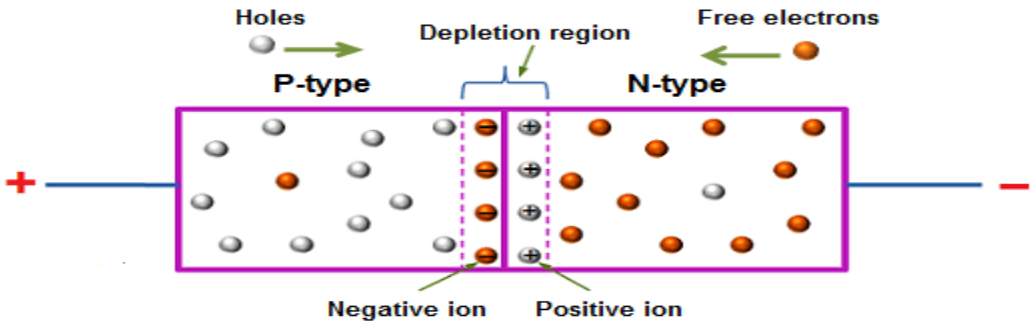
The right hand rising portion is the normal forward biased diode region of the device. The current variation in the vicinity of the origin is due to quantum mechanical tunnelling of electrons through narrow space charge region of the junction. As the applied voltage is increased from zero, tunnelling (current) first increases and then decreases towards zero.



V-I Characteristic of Tunnel Diode

Circuit Globe

This decrease in current with increasing voltage results in a negative resistance region. This region constitute the most useful property of the diode. In this region, the diode instead of absorbing power. Therefore, the tunnel diode can be used as a very high frequency oscillator. When the forward voltage is further increased, the tunnelling effect ceases and current increases in a manner similar to a conventional diode. With the further increase of forward bias, the tunnelling goes on decreasing.



Forward bias tunnel diode

Physics and Radio-Electronics

The current reaches to its minimum value known as valley current ($I_{v)}$ when all the band of filled levels at the bottom of conduction band on N- side is raised to a level corresponding to the forbidden energy gap on P side. When the forward voltage exceeds the valley voltage V_v, the current starts increasing as in case of normal diode. The conventional diode current is also shown in the diode characteristic.

Let us consider the case when the junction is reverse biased. In this case, the filled energy levels of P side become opposite to empty energy levels of N-side because the energy level of P side move up> Now the electrons from the higher energy levels on P side tunnel through the depletion region to lower energy levels on N –side. As a result, significant current flows. On increasing the reverse voltage, the reverse current also increases. It is obvious from the characteristic curve that the reverse characteristic ofd a tunnel diode is linear.

Tunnel diodes are useful in high frequency circuits. There is a very little capacitance associated with the junction and hence the temperature effect are small.

DIAC

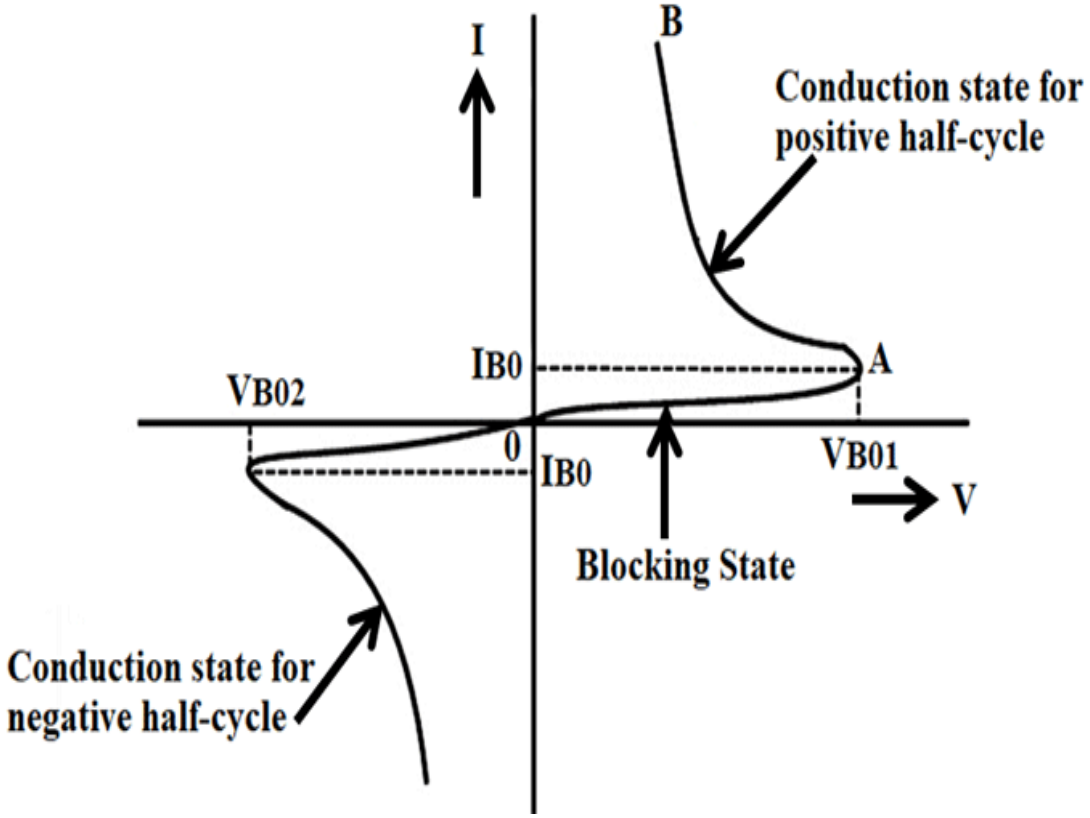
In term DIAC, 'DI' indicates that it is a two terminal device and 'AC' means that the device can be operated on a.c. As DIAC is a bidirectional device. It can be turned ON by either positive or negative half cycle of an a.c voltage.

This is two terminal device having a three semiconductor layers PNP. It has no gate current.

1. There is no base terminal in the DIAC
2. The three regions have almost the same level of doping
3. It gives symmetrical switching characteristics for either polarity of voltages

Let a positive half cycle of a.c is applied. If the applied voltage is less than the forward break over voltage, then a small leakage current flows through the device. The leakage current is produced due to drift of electrons and holes at the depletion region. This current is not sufficient to produce conduction. Therefore, the DIAC remains practically in non-conducting mode. This mode is called as 'blocking mode'. As soon as, the applied voltage, reaches the break over voltage, the device starts conducting. Now, the current through the device starts

increasing. As a result the voltage across it starts decreasing. This is called as conduction ON state.



The DIAC produces symmetrical switching characteristics for both positive as well as negative voltages. Most of the DIACs will be having the breakdown voltage around 30 Volts, the exact breakdown voltage will be based on the type of the device. The DIAC will be in the **conducting state** until the current reaches the particular value called the **holding current**, where holding current is the minimum current that required for a device to keep it in the ON state. When the P-N junction is reverse biased, then any applied voltage of either polarity causes a small saturation current across this junction. It is also obvious from the figure that the DIAC current rises sharply as the applied voltage. In this ON condition, the voltage across the DIAC decr eases with increasing current showing thereby a negative resistance region. The DIAC is used as a trigger device in triac power control systems.

UNIT II

DIGITAL TO ANALOG CONVERTER (D/A CONVERTER)

There are two types of D/A converters.

i)Weighted-Resistor type ii) R- 2R ladder D/A converter.

(i) Weighted-Resistor Type : In it resistance values are weighted in accordance with binary weights (fig. 20, where resistance connected to 2^3 binary weight is $R/2^3$ etc.). With each binary bit, a switch (an electronic) is associated which is closed if the bit is a1 and open if it is a0. Thus logic voltages which represent the individual bits are not applied directly to the converter but are used to operate these electronic switches. In series with these switches weighted resistors are connected. A precise reference voltage line (V_R) is also connected as shown.

When any bit is a1, corresponding switch is closed and corresponding resistor is connected to V_R. The binary number (the digital input) to be converted (held in a resistor) is applied to the switches, so that a current, I, proportional to the binary number (due to weighted resistors) is given out by the arrangement of fig. (20). This current is converted into

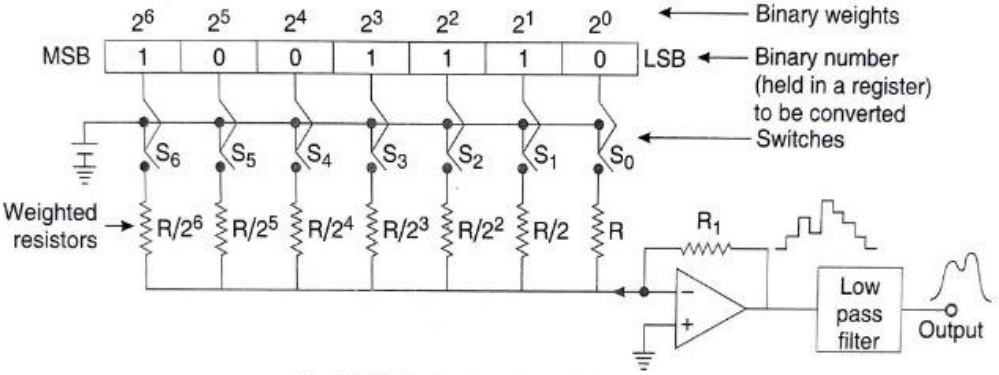


Fig. (20) Weighted resistor *D/A* converter.

output voltage through OP-AMP (being used as current to voltage converter). Thus output voltage is proportional to binary number. As the number gets updated periodically, output voltage will vary as shown in fig. It is then passed through a low pass filter to smooth out the abrupt transitions, giving continuous analog signal.

(ii) R-2R Ladder Type : In above weighted resistor type, we require various value resistors. As the number of bits increases, the ratio of the largest to the smallest resistor goes upto an unconveniently high value, making it difficult to maintain the precision. Errors also creep in due to their temperature dependance. Ladder type overcomes this difficulty by having only two values R and $2R$ of resistors.

Like weighted resistor type, in it too, each bit of binary (held in a resistor) is associated with a switch. As shown in fig. (21), if *MSB* is a1, switch S_3 will connect V_R and the current, I, flowing into the node A, will split into two equal parts at node A. $I/2$ current will flow to the left and $I/2$ to the right. It is because the resistance looking to the right of node A as well as to the left are equal to $2R$ (apply Thevenin conversion). Circuit for $MSB = 1$ is shown in fig. (22). Output of OP-AMP for four stages is given by

$$V_0 = -\frac{R_f\, V_R}{3R}\left(\frac{S_3}{2^1} + \frac{S_2}{2^2} + \frac{S_1}{2^3} + \frac{S_0}{2^4}\right)$$

so that for *MSB*,

$$V_0 = -\frac{R_f\, V_R}{3R}\left(\frac{S_3}{2}\right) = \frac{6R.V_R}{3R}\cdot\frac{1}{2} = -V_R \text{ (if } R_f = 6R) \quad \text{or} \quad \text{gain} \left|\frac{V_R}{V_0}\right| = 1.$$

That is, magnitude of gain from V_R to output is unity for *MSB*. For lower significant bits, current reaching the input of OP-AMP, as a result of successive division, reduces so that gain for n^{th} bit becomes 2^{-n}.

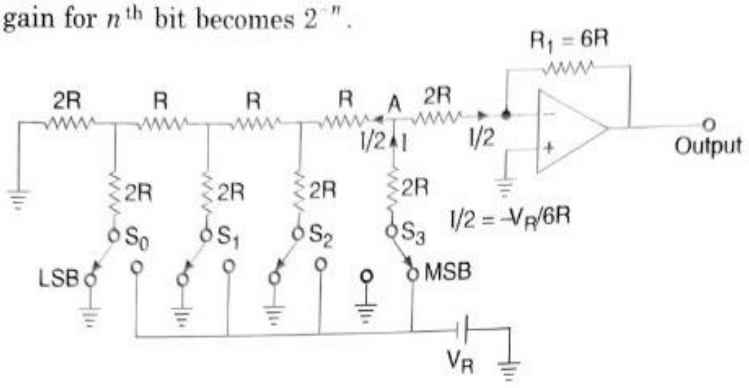


Fig. (21) Ladder type *D/A* converter.

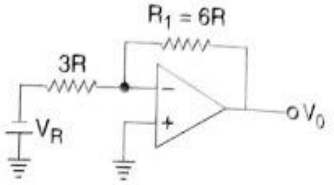


Fig. (22) Circuit for MSB = 1 (on using Thevenin conversion).

19.11 ANALOG TO DIGITAL CONVERTER (A / D CONVERTER) : COUNTER METHOD

Here a counter is allowed to count clock pulses for a duration that is proportional to the amplitude of the analog sample. Thus amplitude of analog sample is quantised in terms of counting of a counter—a digital output. The duration of count is related *linearly* to the sample amplitude through a gate, a comparator and an integrator fig. (23).

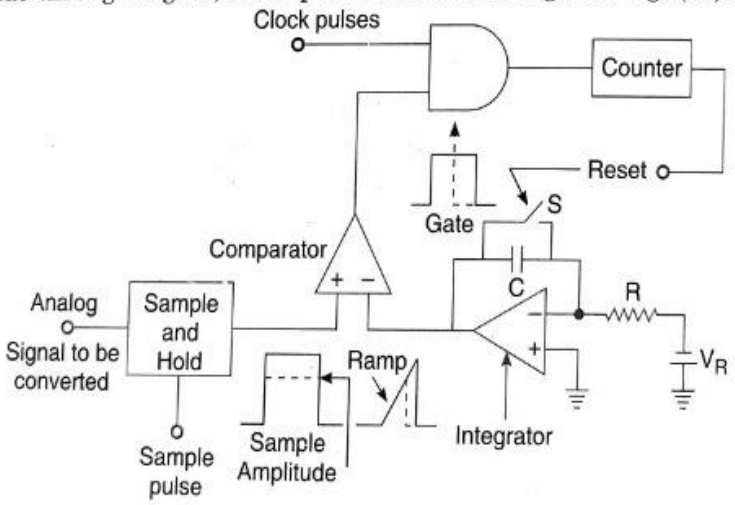


Fig. (23) Ramp type *A / D* converter.

First counter is cleared by applying a reset pulse, and switch, S, across capacitor, C, is momentarily closed and then opened there by resetting the integrator to zero. Now integrator output rises linearly with time (ramp) but as long as it is less than sample amplitude, comparator output is HIGH and therefore allows the clock pulses to go through the AND gate to the counter which counts them. But soon as the integrator output (ramp) becomes greater than sample amplitude, the comparator becomes LOW and the gate is disabled. The counter then stops counting. Thus count accumulated in the counter is linearly related to gate duration, which in its turn, is proportional to the sample amplitude. In other words, counter reading is the digital representation of the sample amplitude. For precision, *ramp should be linear.*

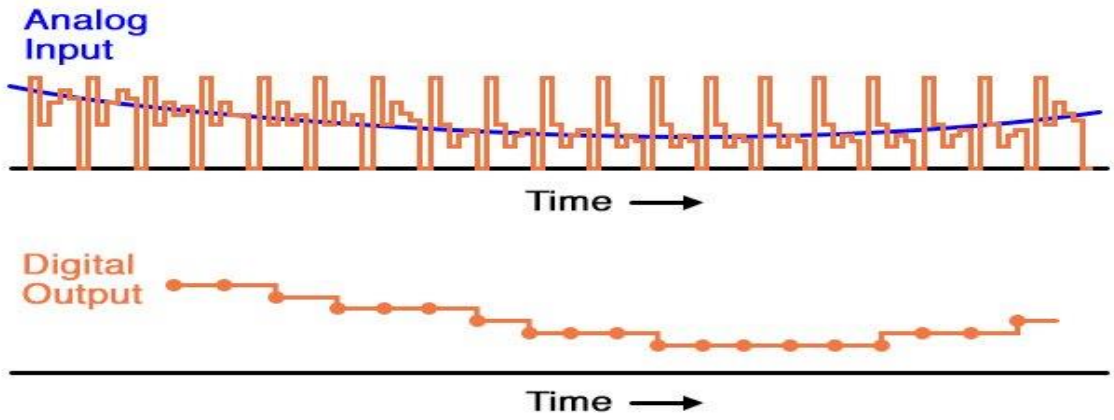
SUCCESSIVE-APPROXIMATION

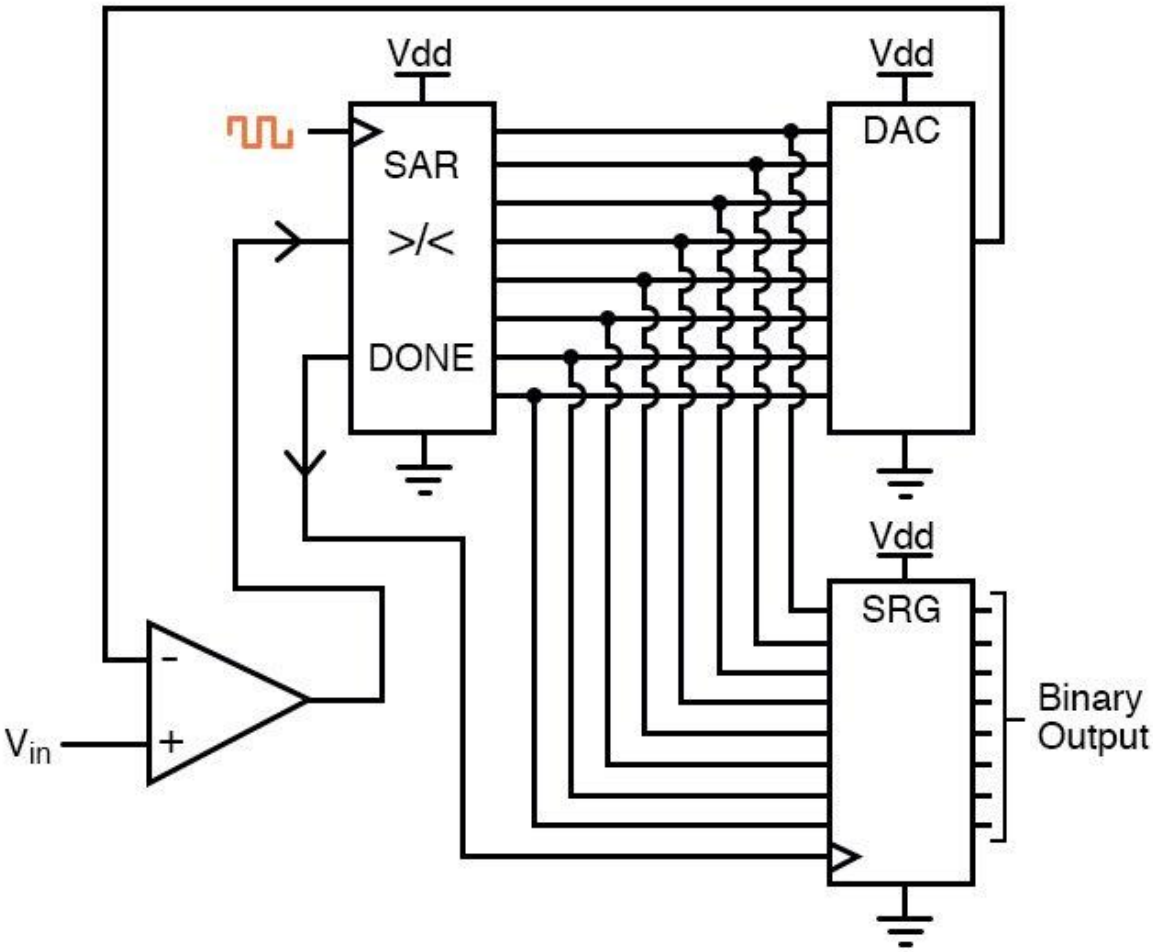
It is one method of addressing the digital ramp ADC's shortcomings. The only change in this design is a very special counter circuit known as a successive-approximation register. Instead of counting up in binary sequence, this register counts by trying all values of bits starting with the most-significant bit and finishing at the least- significant bit.

One method of addressing the digital ramp ADC's shortcomings is the so-called *successive-approximation* ADC. The only change in this design is a very special counter circuit known as *a successive-approximation register*.

Instead of counting up in binary sequence, this register counts by trying all values of bits starting with the most-significant bit and finishing at the least - significant bit. Throughout the count process, the register monitors the comparator's output to see if the binary count is less than or greater than the analog signal input, adjusting the bit values accordingly.

The way the register counts is identical to the "trial-and-fit" method of decimal-to-binary conversion, whereby different values of bits are tried from MSB to LSB to get a binary number that equals the original decimal number. The advantage to this counting strategy is much faster results: the DAC output converges on the analog signal input in much larger steps than with the 0-to-full count sequence of a regular counter.





INVERTING OPERATIONAL AMPLIFIER

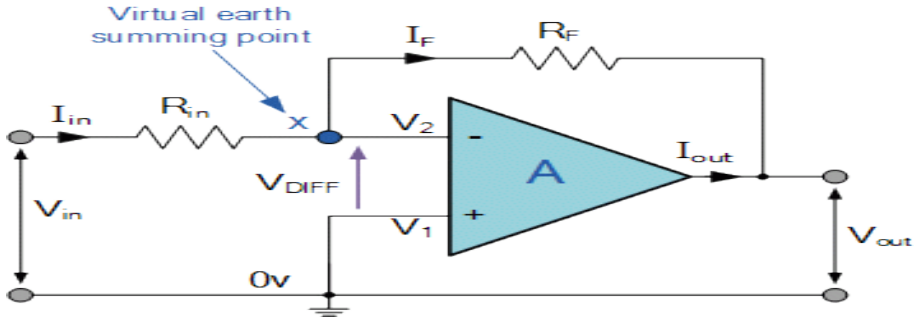
The Inverting Operational Amplifier configuration is one of the simplest and most commonly used op-amp topologies.

Inverting amplifier is one in which the output is exactly 180^0 out of phase with respect to input(i.e. if you apply a positive voltage, output will be negative). Output is an inverted(in terms of phase) amplified version of input.

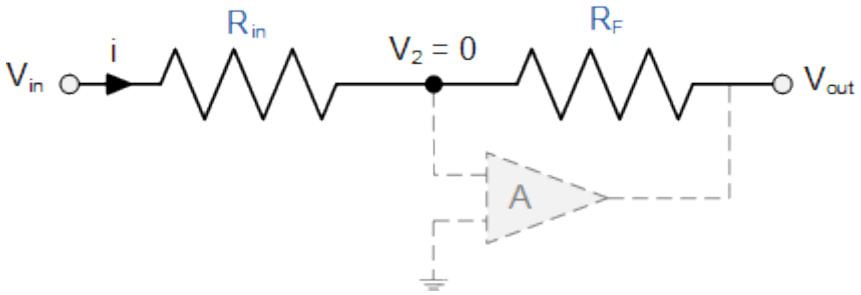
In this **Inverting Amplifier** circuit the operational amplifier is connected with feedback to produce a closed loop operation. When dealing with operational amplifiers there are two very important rules to remember about inverting amplifiers, these are: "No current flows into the input terminal" and that "V1 always equals V2".

- No Current Flows into the Input Terminals

- The Differential Input Voltage is Zero as V1 = V2 = 0 (Virtual Earth)



Current (i) flows through the resistor network as shown.



As the open loop DC gain of an operational amplifier is extremely high we can therefore afford to lose some of this high gain by connecting a suitable resistor across the amplifier from the output terminal back to the inverting input terminal to both reduce and control the overall gain of the amplifier. This then produces and effect known commonly as Negative Feedback, and thus produces a very stable Operational Amplifier based system.

Negative Feedback is the process of "feeding back" a fraction of the output signal back to the input, but to make the feedback negative, we must feed it back to the negative or "inverting input" terminal of the op-amp using an external **Feedback Resistor** called R*ƒ*. This feedback connection between the output and the inverting input terminal forces the differential input voltage towards zero.

This effect produces a closed loop circuit to the amplifier resulting in the gain of the amplifier now being called its **Closed-loop Gain**. Then a closed-loop inverting amplifier uses negative feedback to accurately control the overall gain of the amplifier, but at a cost in the reduction of the amplifiers gain.

$$i = \frac{Vin - Vout}{Rin + Rf}$$

$$\text{therefore, } i = \frac{Vin - V2}{Rin} = \frac{V2 - Vout}{Rf}$$

$$i = \frac{Vin}{Rin} - \frac{V2}{Rin} = \frac{V2}{Rf} - \frac{Vout}{Rf}$$

$$\text{so, } \frac{Vin}{Rin} = V2\left[\frac{1}{Rin} + \frac{1}{Rf}\right] - \frac{Vout}{Rf}$$

$$\text{and as, } i = \frac{Vin - 0}{Rin} = \frac{0 - Vout}{Rf} \qquad \frac{Rf}{Rin} = \frac{0 - Vout}{Vin - 0}$$

$$\text{the Closed Loop Gain (Av) is given as, } \frac{Vout}{Vin} = -\frac{Rf}{Rin}$$

Then, the **Closed-Loop Voltage Gain** of an Inverting Amplifier is given as.

$$\text{Gain (Av)} = \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_{in}}$$

and this can be transposed to give Vout as:

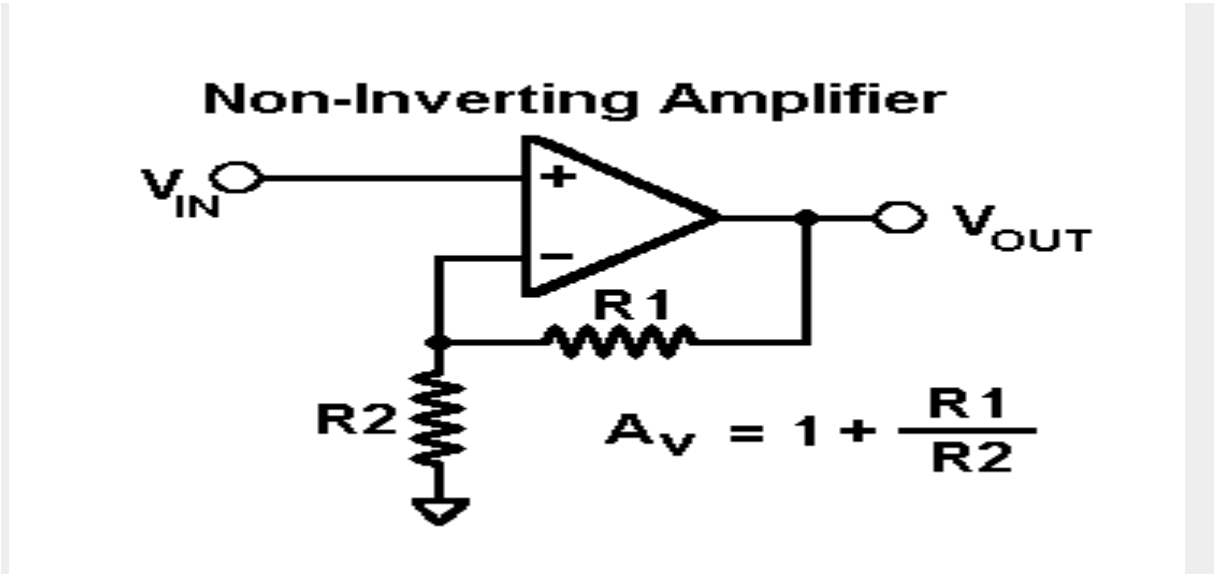
$$Vout = -\frac{Rf}{Rin} \times Vin$$

The negative sign in the equation indicates an inversion of the output signal with respect to the input as it is 180^o out of phase. This is due to the feedback being negative in value.

The equation for the output voltage Vout also shows that the circuit is linear in nature for a fixed amplifier gain as Vout = Vin x Gain. This property can be very useful for converting a smaller sensor signal to a much larger voltage.

Non Inverting amplifier

Non Inverting amplifier is one in which the output is in phase with respect to input(i.e. if you apply a positive voltage, output will be positive). Output is an Non inverted(in terms of phase) amplified version of input.



Feedback control of the non-inverting operational amplifier is achieved by applying a small part of the output voltage signal back to the inverting (–) input terminal via a R*f* – R2 voltage divider network, again producing negative feedback. This closed-loop configuration produces a non-inverting amplifier circuit with very good stability, a very high input impedance, Rin approaching infinity, as no current flows into the positive input terminal, (ideal conditions) and a low output impedance, Rout as shown below. In the previous Inverting Amplifier tutorial, we said that for an ideal op-amp "No current flows into the input terminal" of the amplifier and that "V1 always equals V2". This was because the junction of the input and feedback signal (V1) are at the same potential.

In other words the junction is a "virtual earth" summing point. Because of this virtual earth node the resistors, R*f* and R2 form a simple potential divider network across the non-inverting amplifier with the voltage gain of the circuit being determined by the ratios of R2 and R*f* as shown below.

Then using the formula to calculate the output voltage of a potential divider network, we can calculate the closed-loop voltage gain (A_V) of the **Non-inverting Amplifier** as follows:

$$V_1 = \frac{R_2}{R_2 + R_F} \times V_{OUT}$$

$$\text{Ideal Summing Point: } V_1 = V_{IN}$$

$$\text{Voltage Gain, } A_{(V)} \text{ is equal to: } \frac{V_{OUT}}{V_{IN}}$$

$$\text{Then, } A_{(V)} = \frac{V_{OUT}}{V_{IN}} = \frac{R_2 + R_F}{R_2}$$

$$\text{Transpose to give: } A_{(V)} = \frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_F}{R_2}$$

Then the closed loop voltage gain of a **Non-inverting Operational Amplifier** will be given as:

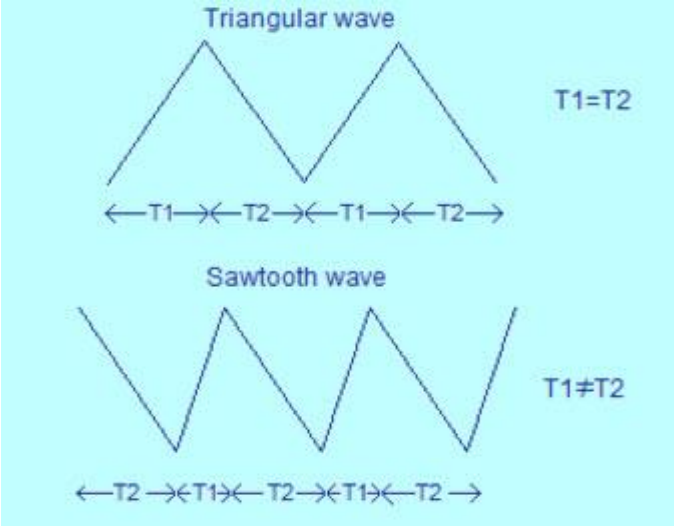
$$A_{(V)} = 1 + \frac{R_F}{R_2}$$

The overall closed-loop gain of a non-inverting amplifier will always be greater but never less than one (unity), it is positive in nature and is determined by the ratio of the values of Rf and R2.

Saw tooth Wave Generator

The saw tooth wave generator is one kind of linear, non sinusoidal waveform, and the shape of this waveform is a triangular shape in which the fall time and rise time are different. The saw tooth waveform can also be named an asymmetric triangular wave.

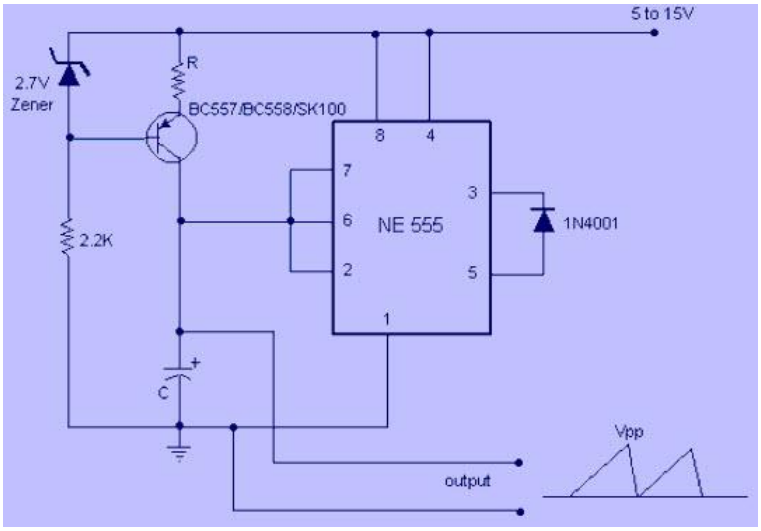
A linear, non-sinusoidal, triangular shape waveform represents a saw tooth waveform in which fall time and rise time are different. A linear, non-sinusoidal, triangular shape waveform represents a pure triangular waveform in which fall time and rise times are equal. The Saw tooth Wave Generator is also known as an asymmetric triangular waveform. The graphical representation of a saw tooth waveform is given below:



The applications of a saw tooth waveform are in frequency/tone generation, sampling, thyristor switching, modulation, etc. A non-sinusoidal waveform is nothing but a saw tooth waveform. Because its teeth look like a saw, it is named as a saw tooth waveform. In an inverse (or reverse) saw tooth waveform the wave suddenly ramps downwards and then rises sharply.

Working Principle of a Saw tooth Wave Generator using 555

A saw tooth wave generator can be constructed using a transistor and a simple 555 timer IC, as shown in the below circuit diagram. It consists of a transistor, a capacitor, a Zener diode, resistors from a constant current source that are used to charge the capacitor. Initially, let us assume that the capacitor is fully discharged. The voltage across the capacitor is zero and the 555's output is high because of the internal comparators connected to the pin 2.



Saw tooth Wave Generator using 555

The capacitor starts charging to supply voltage because the internal transistor of 555 shorting the capacitor to ground and it opens. During charging, the 555 output goes low if the voltage increases above 2/3rd of the supply voltage. During discharging, the 555 output goes high if the voltage across C decreases below 1/3rd supply voltage. Hence the capacitor charges and discharges between 2/3rd and 1/3rd of the supply voltage. But the disadvantage is that it requires a bipolar power supply. The frequency is given by

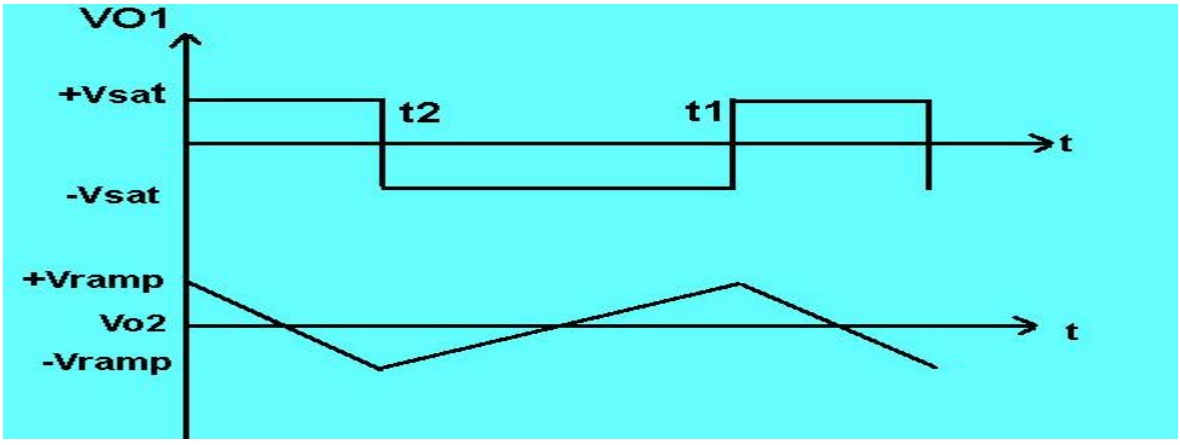
$$\mathbf{F = (Vcc-2.7) / (R*C*Vpp)}$$

Where,

Vpp- Peak to peak output voltage

Vcc- Supply voltage

To get the required frequency value, select the proper values for Vcc, Vpp, R, and C



Then the slope decreases and rise time also decrease. When the comparator output is under positive saturation, the potential difference across the R1 increases and current through

the capacitor resistor also increases. This is due to the presence of a negative voltage at the inverting terminal. Then the slope increases and fall time decreases. And the output is obtained as a saw tooth waveform.

Applications

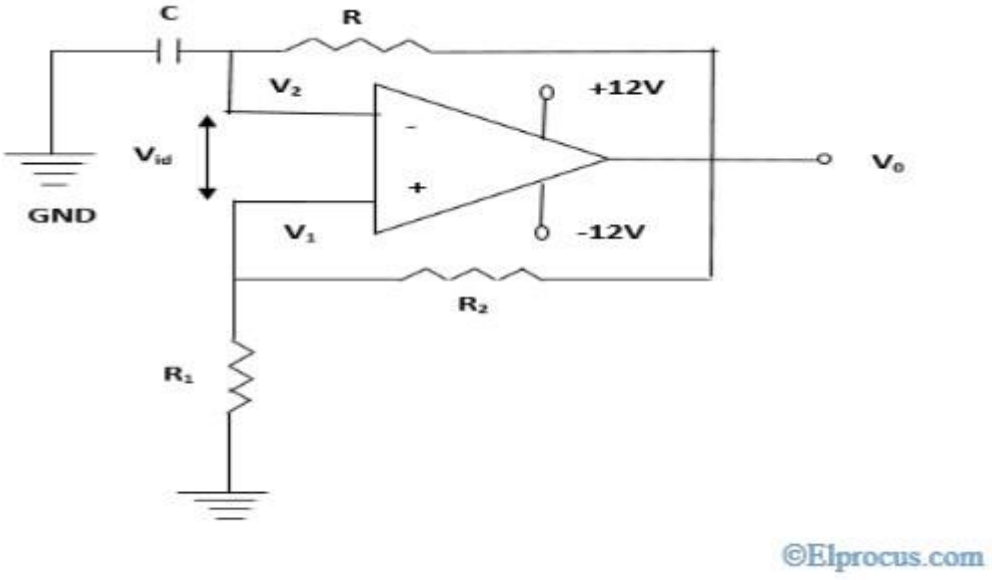
- The saw tooth waveform is the most common waveform used to create sounds with subtractive virtual and analog music synthesizers. Therefore, it is used in music.
- The saw tooth is the form of horizontal and vertical deflection signals that are used to generate a raster on monitor screens or CRT based television.
- The magnetic field suddenly gets collapsed on the wave's cliff, which causes the resting position of its electron beam as quickly as possible.

SQUARE WAVE GENERATOR

The square wave generator is defined as an oscillator that gives the output without any input, without any input in the sense we should give input within zero seconds that means it must be an impulse input. This generator is used in digital signal processing and electronic applications. The square wave generator is also known as Astable Multivibrator or free-running and the frequency of the square wave generator is independent of the output voltage

Square Wave Generator Circuit

To design the square wave generator, we need a capacitor, resistor, operational amplifier, and power supply. The capacitor and resistor are connected to the inverting terminal of the operational amplifier and the resistors R_1 and R_2 are connected to the non-inverting terminal of the operational amplifier. The circuit diagram of the square wave generator using an operational amplifier is shown below



Square Wave Generator Circuit using Op-Amp

If we force output to switch between the positive saturation voltage and the negative saturation voltage at the output of an operational amplifier we can achieve square wave as an output wave. Ideally without any input applied the output should be zero, it is expressed as

V_{out} (output voltage) = 0 V when V_{in} (input voltage) = 0 V
But practically we get some non-zero output that is expressed as

$$V_{0ut} \neq 0$$

The Resistors R_1 and R_2 form a voltage divider network. If the initial output voltage is non-zero we get voltage across V_b. Thus we get a positive input at the non-inverting terminal and the inverting terminal, then the output gets amplified by its gain and reaches the maximum output voltage thus we get the half of the square wave as shown in figure

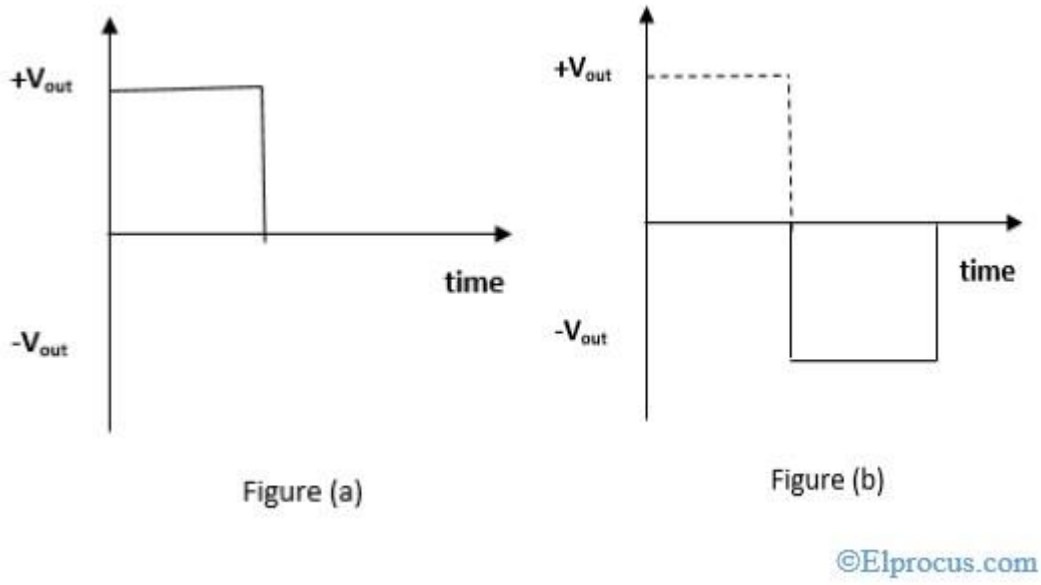
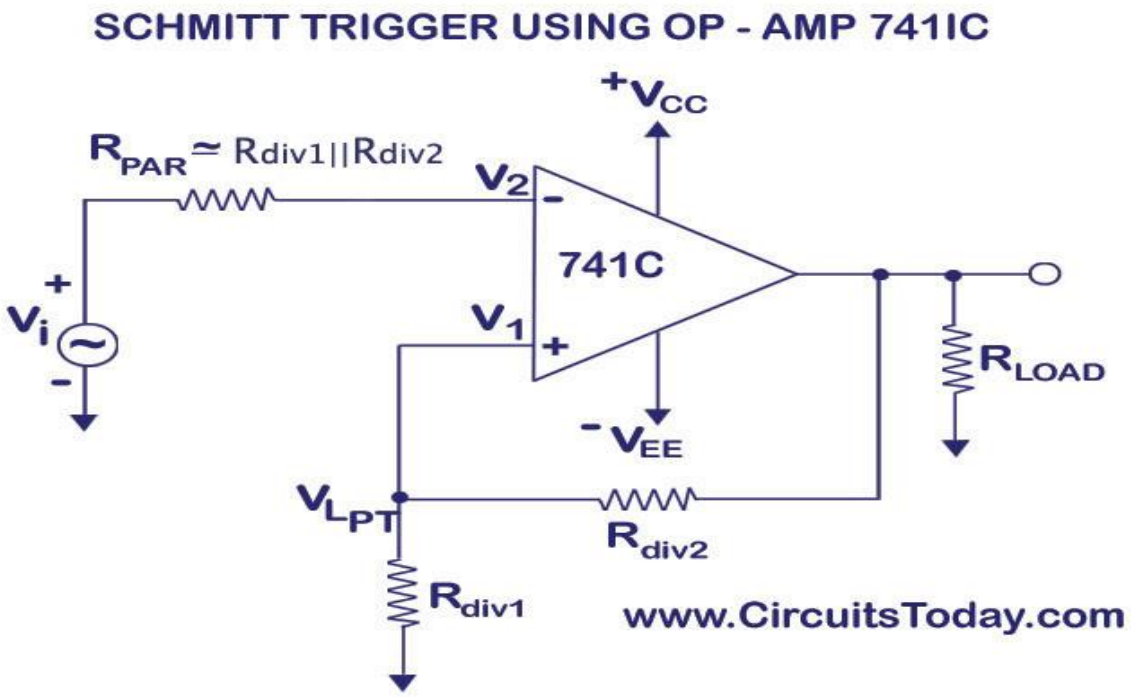


Figure (a) Figure (b)

The capacitor starts charging when we have a non-zero input at the inverting terminal. It will charge continuously until its voltage become greater than V_b. As soon as V_c is greater than the V_b ($V_c > V_b$). The inverting input becomes greater than the non-inverting input and hence op-amp output switches to negative voltage and gets amplified till $(-V_{out})_{max.}$ Thus will get the negative half of the square wave as shown in figure (b). This is the application of an op-amp as a square wave generator.

Schmitt trigger

A **Schmitt trigger** is a comparator (not exclusively) circuit that makes use of positive feedback (small changes in the input lead to large changes in the output in the same phase) to implement hysteresis (a fancy word for delayed action) and is used to remove noise from an analog signal while converting it to a digital one.



A **Schmitt trigger** makes use of **positive feedback** – it takes a sample of the output and feeds it back into the input so as to 'reinforce', so to speak, the output – which is the exact opposite to negative feedback, which tries to nullify any changes to the output.

Assume the input voltage is lower than the reference voltage at the non-inverting pin and the output is therefore high.

V* is the reference input voltage which creates a fixed bias at the non-inverting input. Since the output is high through the pullup resistor, this creates a current path through the feedback resistor, slightly increasing the reference voltage.

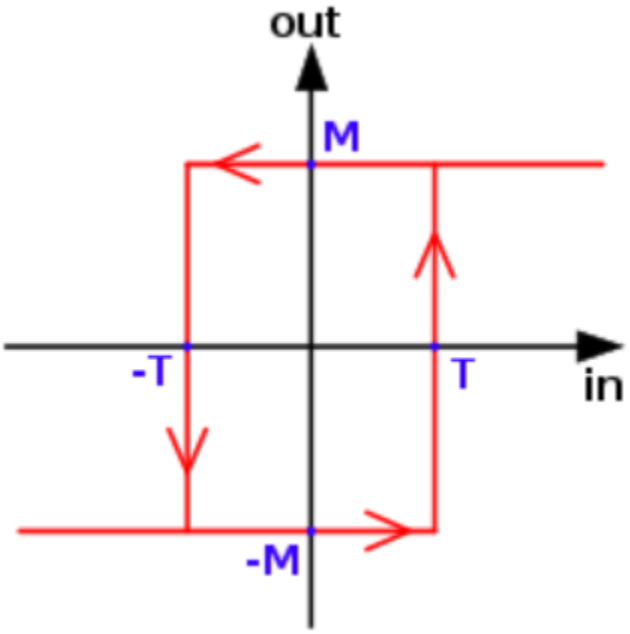
When the input goes above the reference voltage, the output goes low. Normally this shouldn't affect the reference voltage in any way, but since there's a feedback resistor, the reference voltage drops slightly below the nominal value because the feedback and the lower reference resistor are now in parallel with respect to ground (since a low output shorts that terminal of the resistor to ground). Since the reference voltage is lowered, there is no chance of a small change in input causing multiple transitions – in other words, there is no longer a dead zone.

To cause the output to go high, the input must now cross the new lower threshold. Once crossed, the output goes high and the circuit is 'reset' to the initial configuration. The input has to cross the threshold just once resulting in a single clean transition. The circuit now has two effective thresholds or states – it is bistable.

This can be summarised in the form of a graph:

$$f \approx \frac{1}{RC \ \ell n \dfrac{V_{T+}(V_{DD} - V_{T-})}{V_{T-}(V_{DD} - V_{T+})}}$$

Where R and C are the resistance and capacitance, V_T+ is the upper threshold, V_T- is the lower threshold and V_{DD} is the supply voltage.

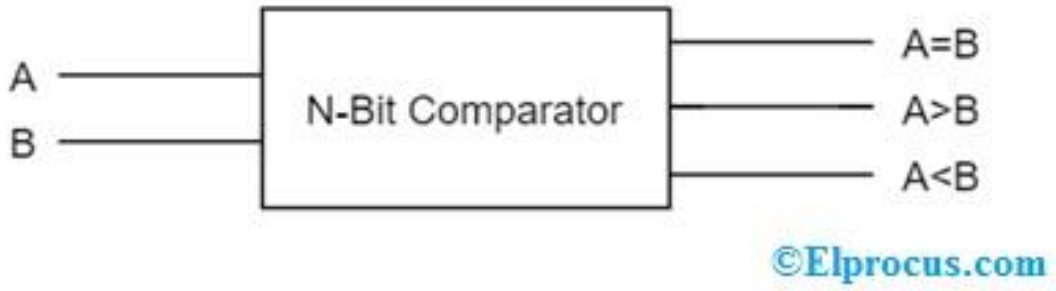


UNIT III

Digital Comparator

A data comparison is mostly required in many digital systems at the time of logical or arithmetic functions, digital comparators are the one best option to compare data. Digital comparators are the most appropriate combinational logic circuits used to compare relative magnitudes of two binary numbers.

A comparator that compares two binary bits and produces three outputs based on the relative magnitudes of given binary bits is called a 1-bit magnitude comparator.



The device accepts two binary numbers (A and B)as input and generates an output based on the magnitude of given inputs (example: A=B or A>B or A<B). Digital Comparators are developed through logic gates like AND, NOT or NOR gates. Digital comparators are available as identity comparators and magnitude comparators.

A comparator that compares two binary bits and produces three outputs based on the relative magnitudes of given binary bits is called a 1-bit magnitude comparator.

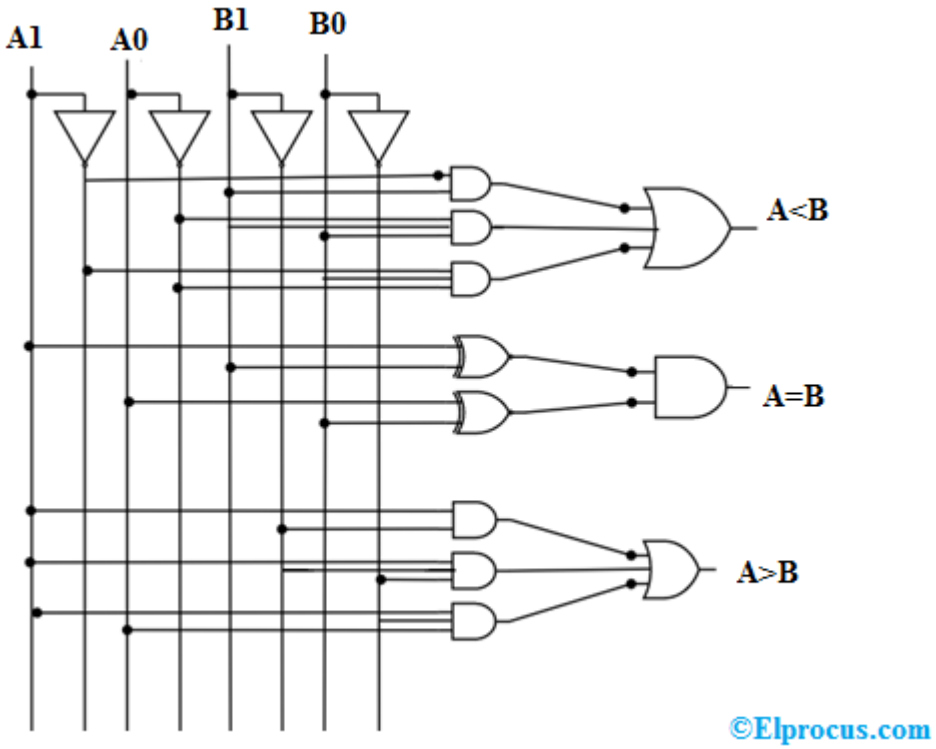
2-bit Magnitude Comparator

A comparator that compares two binary numbers (each number having 2 bits) and produces three outputs based on the relative magnitudes of given binary bits is called a 2-bit magnitude comparator.

The truth table derives the expressions of A<B, A>B, and A=B as below

A<B – A1'B1'+ A0'B1B0 + A1'A0'B0
A>B – A1B1' + A0B1'B0' + A1A0B0'
A=B – (A0 Ex-Nor B0) (A1 Ex-Nor B1)

A	B	A<B	A>B	A=B
0	0	0	0	1
0	1	1	0	0
1	0	0	1	0
1	1	0	0	1



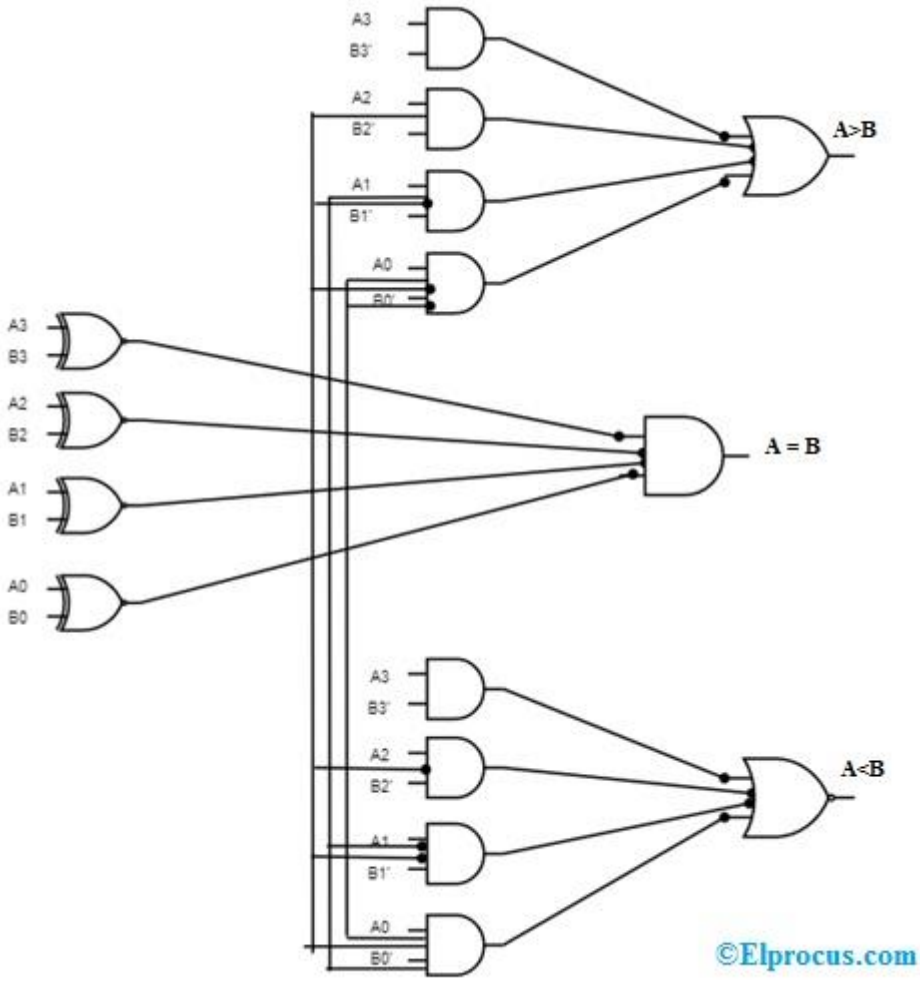
4-bit Magnitude Comparator

A comparator that compares two binary numbers (each number having 4 bits) and produces three outputs based on the relative magnitudes of given binary bits is called a 4-bit magnitude comparator.

The input bits can be termed as **A = A3 A2 A1 A0** and **B = B3 B2 B1 B0**
The output is **A> B** in the cases of
A3 = 1 and **B3 = 0**
A3 = B3 and **A2 = 1, B2 = 0**
A3 = B3 and **A2= B2** and **A1 = 1** and **B1 = 0**
A3 = B3 and **A2= B2** and **A1 = B**1 and A0 = 1 and **B0 = 0**
And **A>B** can be expressed as
A>B = A3B3' + (A3 Ex-Nor B3) A2B2' + (A3 Ex-Nor B3) (A2 Ex-Nor B2) A1B1' + (A3 Ex-Nor B3) (A2 Ex-Nor B2) (A1 Ex-Nor B1) A0B0'
While

A<B = A3'B3 + (A3 Ex-Nor B3) A2'B2 + (A3 Ex-Nor B3) (A2 Ex-Nor B2) A1'B1 + (A3 Ex-Nor B3) (A2 Ex-Nor B2) (A1 Ex-Nor B1) A0'B0
And similarly, A=B can be expressed as

A=B = (A3 Ex-Nor B3) (A2 Ex-Nor B2) (A1 Ex-Nor B1)(A0 Ex-Nor B0)
With these expressions, the Circuit diagram can be as follows.



Mostly, 4-bit comparators are in the form of IC's and the IC 7485 is widely used. Data comparison can be performed by grounding A>B, A<B and A+B inputs to the Vcc terminal. Furthermore, this integrated circuit performs a cascading operation where it helps for cascading multiple comparators.

Applications Comparator

Digital comparator and magnitude comparator is used in different applications where data comparison is mostly required in many of the activities, and these hold many benefits too.

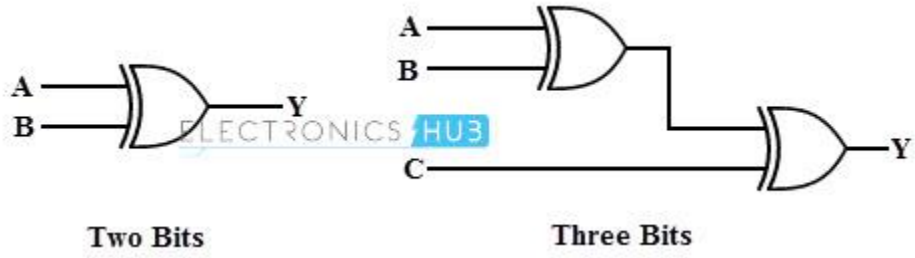
- Used for authorization purposes (such as password management) and biometric applications.
- These are implemented in process controllers and also in servo motor controls.
- Implemented for the data comparison of variables like temperature, the pressure is compared with that of reference values.
- Used to address decoding circuitry in computers.

Parity generator and checker

A parity generator is a combinational logic circuit that generates the parity bit in the transmitter. On the other hand, a circuit that checks the parity in the receiver is called parity checker. A combined circuit or devices of parity generators and parity checkers are commonly used in digital systems to detect the single bit errors in the transmitted data word.

The sum of the data bits and parity bits can be even or odd . The basic principle involved in the implementation of parity circuits is that sum of odd number of 1s is always 1 and sum of even number of 1s is always zero. Such error detecting and correction can be implemented by using Ex-OR gates (since Ex-OR gate produce zero output when there are even number of inputs).

To produce two bits sum, one Ex-OR gate is sufficient whereas for adding three bits two Ex-OR gates are required as shown in below figure.



In even parity bit scheme, the parity bit is '**0**' if there are even number of 1s in the data stream and the parity bit is '**1**' if there are odd number of 1s in the data stream.

In odd parity bit scheme, the parity bit is '**1**' if there are even number of 1**s** in the data stream and the parity bit is '**0**' if there are odd number of 1s in the data stream. Let us discuss both even and odd parity generators.

3-bit message			Even parity bit generator (P)
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Even Parity Checker

Consider that three input message along with even parity bit is generated at the transmitting end. These 4 bits are applied as input to the parity checker circuit which checks the possibility of error on the data. Since the data is transmitted with even parity, four bits received at circuit must have an even number of 1s.

If any error occurs, the received message consists of odd number of 1s. The output of the parity checker is denoted by PEC (parity error check).

The below table shows the truth table for the even parity checker in which PEC = 1 if the error occurs, i.e., the four bits received have odd number of 1s and PEC = 0 if no error occurs, i.e., if the 4-bit message has even number of 1s.

4-bit received message				Parity error check C_p
A	B	C	P	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Odd Parity Checker

Consider that a three bit message along with odd parity bit is transmitted at the transmitting end. Odd parity checker circuit receives these 4 bits and checks whether any error are present in the data. If the total number of 1s in the data is odd, then it indicates no error, whereas if the total number of 1s is even then it indicates the error since the data is transmitted with odd parity at transmitting end.

The below figure shows the truth table for odd parity generator where **PEC =1** if the 4-bit message received consists of **even number of 1s** (hence the error occurred) and **PEC= 0** if the message contains **odd number of 1s** (that means no error).

4-bit received message				Parity error check C_p
A	B	C	P	
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

19.4 THE J - K FLIP FLOP

A J-K flip flop is a refinement of RS flip flop in that the indeterminate state of the RS flip flop, namely, inputs $R = S = 1$ or $\overline{R} = \overline{S} = 0$ giving rise to uncertain output Q_{n+1}, is well defined in this flip flop. A slight additional circuitry to the clocked RS flip-flop is necessary to achieve J-K operation. Refer to fig. (1) of Art. 19·1, where we have represented a SR flip flop symbolically. If we insert clock in it then $RS \mid T$ flip flop is shown in fig. (8a).

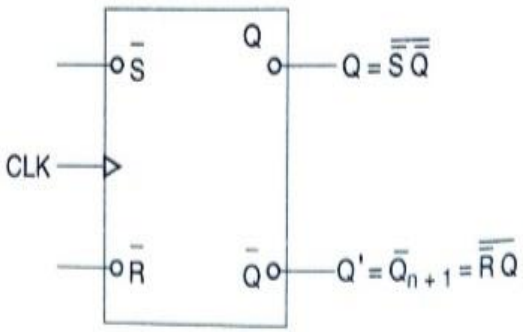


Fig. (8a) A S-R flip flop.

In it we add two NAND gates with :

(i) Inputs J and $\overline{Q}$ (fedback from output) to NAND gate, connected to $\overline{S}$, and

(ii) inputs K and Q (fedback from output) to NAND gate connected to $\overline{R}$.

Therefore circuit of J-K flip flop looks as shown in fig. (8b).

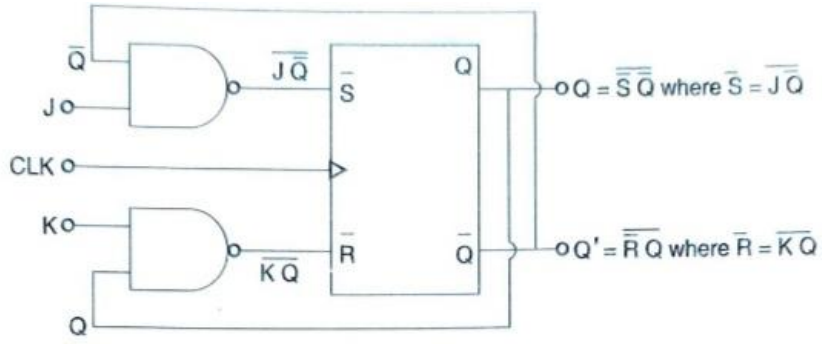


Fig. (8b) J-K flip flop.

We note from fig. (8b) that there are cross connections from output to J-K inputs. $\overline{Q}$ is connected to J input while Q is connected to K input. Inputs J and K behave like inputs S and R to SET and RESET (clear) the flip flop. In J-K flip flop letter J is for SET and letter K is for RESET.

The output of JK flip flop is

$$Q = \overline{\overline{S}\ \overline{Q}} \quad \text{with} \quad \overline{S} = \overline{J\,\overline{Q}} \qquad \ldots 1(a)$$

and

$$\overline{Q} = Q' = \overline{\overline{R}\ Q} \quad \text{with} \quad \overline{R} = \overline{KQ} \qquad \ldots 1(b)$$

Combining the two, the characteristic equation for the flip flop [putting eq. 1(b) in eq. 1(a) and using De Morgan's theorem] is

$$Q = \overline{\overline{S}\ \overline{\overline{R}Q}} = \overline{\overline{S}} + \overline{\overline{\overline{R}\,Q}} = S + \overline{R}\,Q \qquad \text{see art. 19·1} \quad \ldots(2)$$

As in J-K flip flop $\overline{S} = \overline{J\,\overline{Q}}$ So $S = J\,\overline{Q}$

and $\overline{R} = \overline{KQ} = (\overline{K} + \overline{Q})$, De morgan's Theorem

we get from eq. (2) that

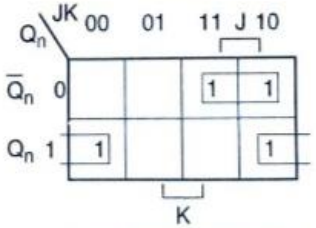
$$\begin{aligned} Q &= J\,\overline{Q} + (\overline{K} + \overline{Q})\,Q \\ &= J\,\overline{Q} + \overline{K}\,Q + Q\,\overline{Q} \\ &= J\,\overline{Q} + \overline{K}\,Q \end{aligned}$$

This gives the characteristic equation for JK flip flop and in terms of present and next output (states), it can be written as

$$\boxed{Q_{n+1} = J_n\,\overline{Q}_n + \overline{K}_n\,Q_n}$$

This characteristic equation leads to the transition table for J-K flip flop, shown in fig. (8c).

Q_n Present State	J	K	Q_{n+1} Next State	
0	0	0	0	
1	0	0	1	
0	0	1	0	
1	0	1	0	
0	1	0	1	
1	1	0	1	
0	1	1	1 ←	Well defined
1	1	1	0 ←	Well defined



Characteristic equation :
$Q_{n+1} = J\,\overline{Q}_n + \overline{K}\,Q_n$

Fig. (8c)

Let us see for indeterminate state of RS/T flip flop. Here input $J = K = 1$ are allowed as output state is now well defined and not uncertain. Let us, for example, take that prior to the application of clock pulse,

$$Q = 0 \qquad \text{and} \qquad \overline{Q} = 1$$

That is, if present state is

$$Q_n = 0 \qquad \text{and} \qquad \overline{Q}_n = 1$$

Then next state with $J = K = 1$ input from characteristic equation will be

$$Q_{n+1} = J_n \overline{Q}_n + \overline{K}_n Q_n$$
$$= 1.1 + 0.\overline{1} = 1.1 + 0.0 = 1$$

which is well defined. Or if the present state is

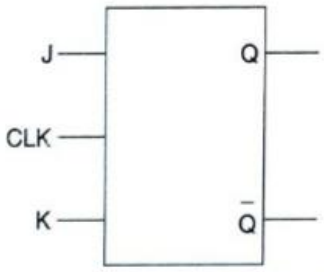
$$Q_n = 1 \qquad \text{and} \qquad \overline{Q}_n = 0$$

then next state for $J = K = 1$ input,

$$Q_{n+1} = J_n \overline{Q}_n + \overline{K}_n Q_n$$
$$= 1.\overline{1} + \overline{1}.1 = 1.0 + 0.1 = 0$$

which is well defined. These are shown in the transition table.

Symbolically fig. (8b) of J-K flip flop and its transition table can be represented as shown in fig. (8d).



J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

Fig. (8d)

The complete gate circuit of fig. (8b) of J-K flip flop with present and clear direct inputs can be traced as shown in fig. (8e).

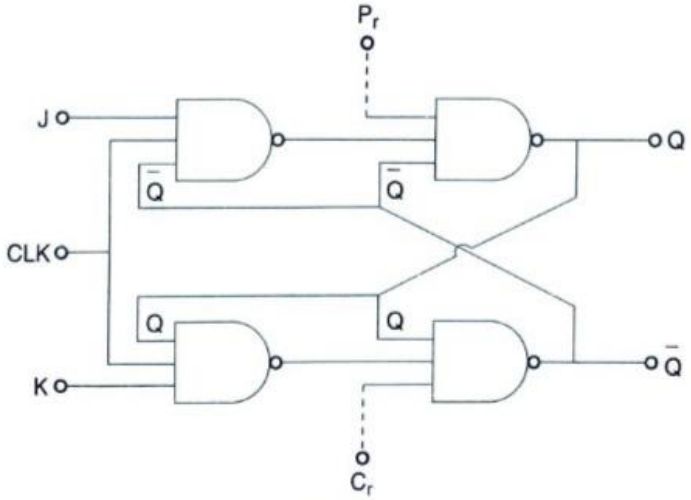


Fig. (8e)

Drawback of J-K Flip Flop : Race Around Condition : The difficulty with *J-K* flip flop is that flip flop continues to operate for the whole duration t_p of clock pulse (because it is level sensitive). It means when $J = K = 1$ and CLK = 1 (HIGH) for duration, t_p, the output will continue to change from $\overline{Q}$ to Q then Q to $\overline{Q}$ ($0 \rightarrow 1$ and then $1 \rightarrow 0$). This oscillating output is called race around condition.

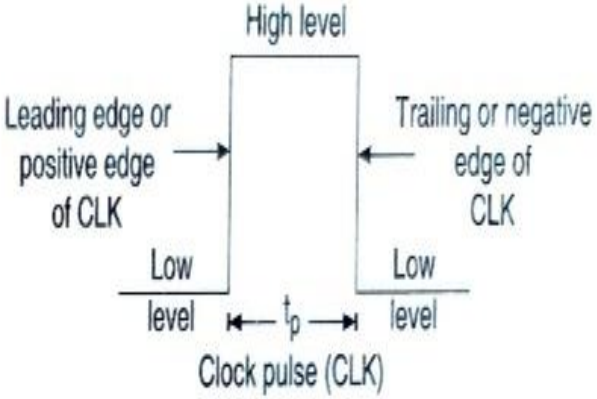


Fig. (8f)

This type of rapid transition of output states is undesirable. This can be avoided in two ways :

(1) It can be made edge sensitive. That is flip flop should operate only at the leading edge or trailing edge of the pulse (then called edge trigered) so that operation is instantaneous, or

(2) Two separate units of flip flop should be used one for input and other for output. When one unit, say input FF operates, output flip flop unit *should not* operate (inhibited) so that output Q and $\overline{Q}$ do not change when input unit is operating. This arrangement is called master-slave *J-K* flip flop. Thus when $J = K = 1$, input will change only if outputs Q and $\overline{Q}$, being fed back to input, change from $1 \rightarrow 0$ and $0 \rightarrow 1$. So if Q and $\overline{Q}$ do not change, input will not change and the output will be definite.

(A) Decoder : In digital systems, instructions as well as numbers are conveyed by means of binary levels or pulse trains. In BCD (Art. 18·4) we use a 4-bit character. The 4-bit in binary can be arranged in 16 distinct ways and therefore 16 different instructions can be coded (16 codes) in a binary form. We may design the circuit in such a way that for each of the 16 codes, one and only one line is to be excited. This process of identifying particular code is called decoding.

Suppose a decoder fig. (34) produces 1 output only for a BCD input of 1001 (equivalent to decimal 9) [note that in BCD, binary numbers are from 0000 to 1001 (art. 21.4) and number 1010 through 1111 cannot occur for normal opearation] so that truth table is as

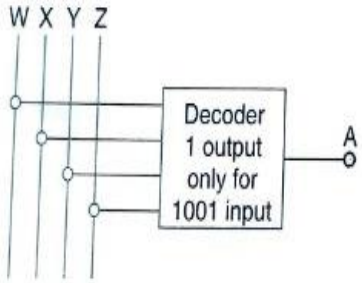


Fig. (34)

W	X	Y	Z	A
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1

Fig. (35) Ten in all. 9-zero 1-one. ⁻⁹ee K-map.

shown in fig. (35). We use Karnaugh map to find the logic circuit in ıe decoder of fig. (34), We have 1 output only for one input condition

$$WXYZ = 1001$$

Referring to fig. (36a), the fundamental product for this is $W\,\overline{X}\,\overline{Y}\,Z$. Fig. (36a) also shows '0's corresponding to other input conditions of the truth table. The empty spaces refer to the forbidden *BCD* inputs, not listed in the truth table.

	$\overline{Y}\overline{Z}$	$\overline{Y}Z$	YZ	$Y\overline{Z}$
$\overline{W}\overline{X}$	0	0	0	0
$\overline{W}X$	0	0	0	0
WX				
$W\overline{X}$	0	1		

(a)

	$\overline{Y}\overline{Z}$	$\overline{Y}Z$	YZ	$Y\overline{Z}$
$\overline{W}\overline{X}$	0	0	0	0
$\overline{W}X$	0	0	0	0
WX	X	X	X	X
$W\overline{X}$	0	1	X	X

(b)

	$\overline{Y}\overline{Z}$	$\overline{Y}Z$	YZ	$Y\overline{Z}$
$\overline{W}\overline{X}$	0	0	0	0
$\overline{W}X$	0	0	0	0
WX	X	X	X	X
$W\overline{X}$	0	1	X	X

(c)

Fig. (36)

Since forbidden *BCD* inputs do not occur under normal operating conditions, *these empty space of K-map can be treated as '0's or '1's whichever is more convenient and mark them by* × *the don's care conditions* fig. (36b). We can use these '×' to the best possible advantage by following these ideas :

(i) Enter '1's on K-map for fundamental products that produce output '1's in the truth table. Enter '0's for the other inputs listed in the truth table, and enter '×' for the forbidden inputs.

(ii) Encircle the actual '1's on the K-map in the largest groups we can find by treating the don't care conditions as '1's.

(iii) After actual '1's have been included in groups, disregard the remaining don't cares by visualising them as '0's.

Thus, as pointed out in point (ii) above, we include 1 in a *quad* fig. (36c) and form the largest group by visualising all '×'s (that are included in the quad) as '1's. Therefore Boolean equation will be

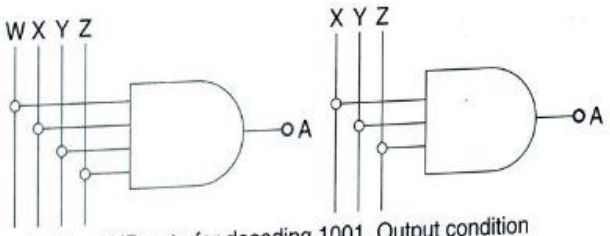
$$A = WX\,\overline{Y}\,Z + WXYZ + W\,\overline{X}\,\overline{Y}\,Z + W\,\overline{X}\,YZ.$$

Because X and Y have been complemented, they drop out and therefore reduced expression is

$$A = WZ$$

which is the output of an AND gate fig. (37a), which gives that when W and Z both are '1's (which happens only for a BCD input of 1001) the output A equal a 1.

Decoding 0111 : The simplest logic circuit for decoding a BCD input of 0111 as a 1 output is shown in fig. (37b), with K-map. The fundamental product is $\overline{W}\,X\,Y\,Z\,(=1)$. The



(a) An AND gate for decoding 1001. Output condition X, Y, Z are activated lines

	$\overline{Y}\overline{Z}$	$\overline{Y}Z$	YZ	$Y\overline{Z}$
$\overline{W}\overline{X}$	0	0	0	0 (WXYZ=1)
$\overline{W}X$	0	0	1	0
WX	X	X	X	X
$W\overline{X}$	0	0	X	X

(b) Decoding 0111

Fig. (37)

most efficient way to encircle is to group 1 into a *pair* using the don't care as shown. Since this is the largest group possible, all other don't care are treated as '0's. The equation for the pair is

$$A = X\,Y\,Z$$

The three input gate produces a 1 output only for a BCD input of 0111.

(B) Encoder : It performs a reverse decoder function. An encoder accepts a digit on its inputs, such as a decimal digit and converts it to a coded output, such as binary or BCD.

We shall describe the decimal to BCD encoder. From table for BCD code, we note that:

(i) Most significant bit (MSB) of BCD code is D and it is a 1 for decimal digits 8 or 9. The expression for bit D interms of decimal digits can therefore be written as

$$D = 8 + 9 \qquad \ldots(1)$$

(ii) Bit C of BCD code is a 1 for decimal digits 4, 5, 6, 7 so that

$$C = 4 + 5 + 6 + 7 \qquad \ldots(2)$$

(iii) Bit B is a 1 for decimal digits 2, 3, 6 or 7 so that

$$B = 2 + 3 + 6 + 7 \qquad \ldots(3)$$

(iv) Bit A is a 1 for decimal digits 1, 3, 5, 7 or 9. The expression for A is

$$A = 1 + 3 + 5 + 7 + 9 \qquad ...(4)$$

Basic logic for a decimal to BCD encoder is shown in fig. (38). From logic we note that :

(i) if a high (a 1) occurs at input decimal digit 7 line then it will produce a high (a1) at

Decimal digit	BCD code			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

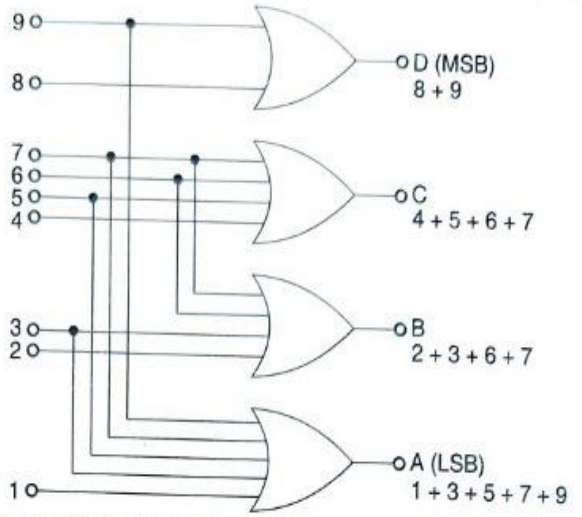


Fig. (38) Basic logic for a decimal to BCD encoder.

output lines C, B and A (see eqs. 2, 3, 4 as 7 occur in C, B, A) and a low (a0) at D so that for input decimal digit 7 we get an output DCBA = 0111, the BCD code for decimal digit 7.

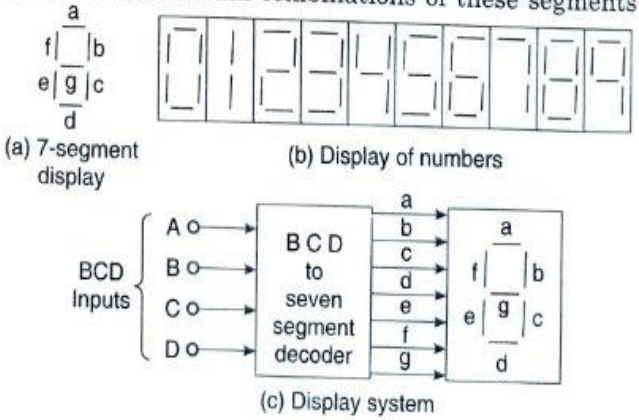
(ii) if a high (a1) occurs at input decimal digit 9 line then it will produce a high (a1) at output lines D and A (see eqs. 1, 4 as 9 occurs in D and A only) and rest output lines (*i.e.* B and C) will be at a low (a0) so that for input decimal 9, we shall get an output DCBA = 1001.

Similarly for other decimal digits. Thus we conclude that when a *high* appears on one of the decimal digit input lines, the appropriate level occurs on the four BCD output lines.

18.13 BCD-TO-7 SEGMENT DECODER

Such a type of decoder consists 7 LED (light emitting diode) segments which, as shown in fig. (39a), display decimal numerals 0 to 9 when certain combinations of these segments are lighted. To produce 1, segments f and e are illuminated, to produce a 2, segments a, b, g, e and d are used, etc., fig. (39b). When a particular light emitting diode is forward biased, it conducts current and then light is emitted. Thus that particular segment is illuminated.

The truth table for BCD-to-7 segment decoder is given in table-1. Here ABCD is the natural BCD code for numerals 0 through 9.



(a) 7-segment display

(b) Display of numbers

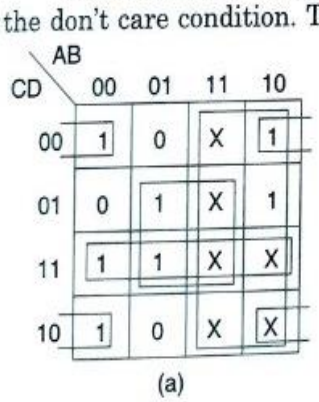
(c) Display system

Fig. (39)

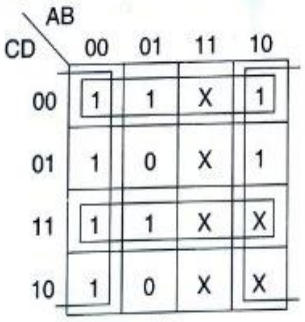
Table–1 : Truth Table of BCD-to-7 Segment Decoder

Decimal digit displayed	Inputs				Outputs						
	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	0	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	0	0	1	1

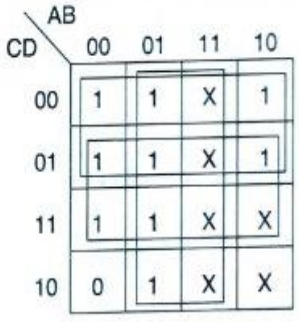
The K-maps for each of the outputs a through g are given in fig. (40). Cross, ×, refers to the don't care condition. These are the entries corresponding to six binary combinations not



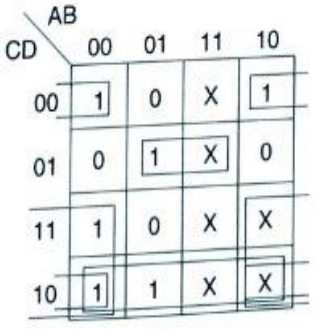
(a)



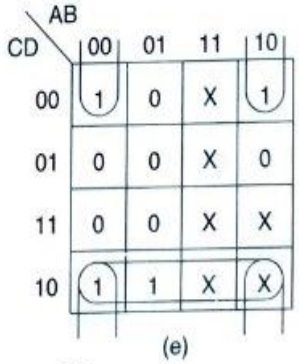
(b)



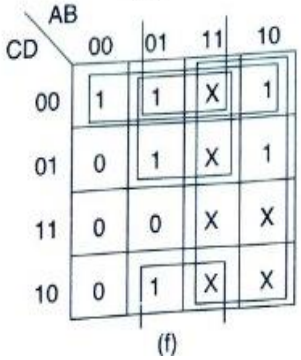
(c)



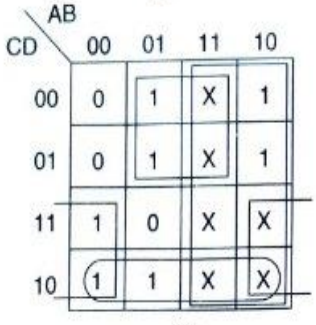
(d)



(e)



(f)



(g)

used in the truth table (*e.g.* there is no 1100, 1101, 1111, 1110, 1011, 1010 in the truth table. So in their place, a cross × has been put). The K-maps are simplified and the minimum expression are given by

$$a = \overline{B}\,\overline{D} + B\,D + C\,D + A \quad \ldots(1)$$

$$b = \overline{B} + \overline{C}\,\overline{D} + C\,D \quad \ldots(2)$$

$$c = B + \overline{C} + D = \overline{\overline{B}\,C\,\overline{D}} \quad \ldots(3)$$

$$d = \overline{B}\,\overline{D} + C\,\overline{D} + \overline{B}\,C + B\,\overline{C}\,D \quad \ldots(4)$$

$$e = \overline{B}\,\overline{D} + C\,\overline{D} \quad \ldots(5)$$

$$f = A + \overline{C}\,\overline{D} + B\,\overline{C} + B\,\overline{D} \quad \ldots(6)$$

$$g = A + B\,\overline{C} + \overline{B}\,C + C\,\overline{D} \quad \ldots(7)$$

Realisation of eqs. (1) to (7) is done through NAND gates fig. (41).

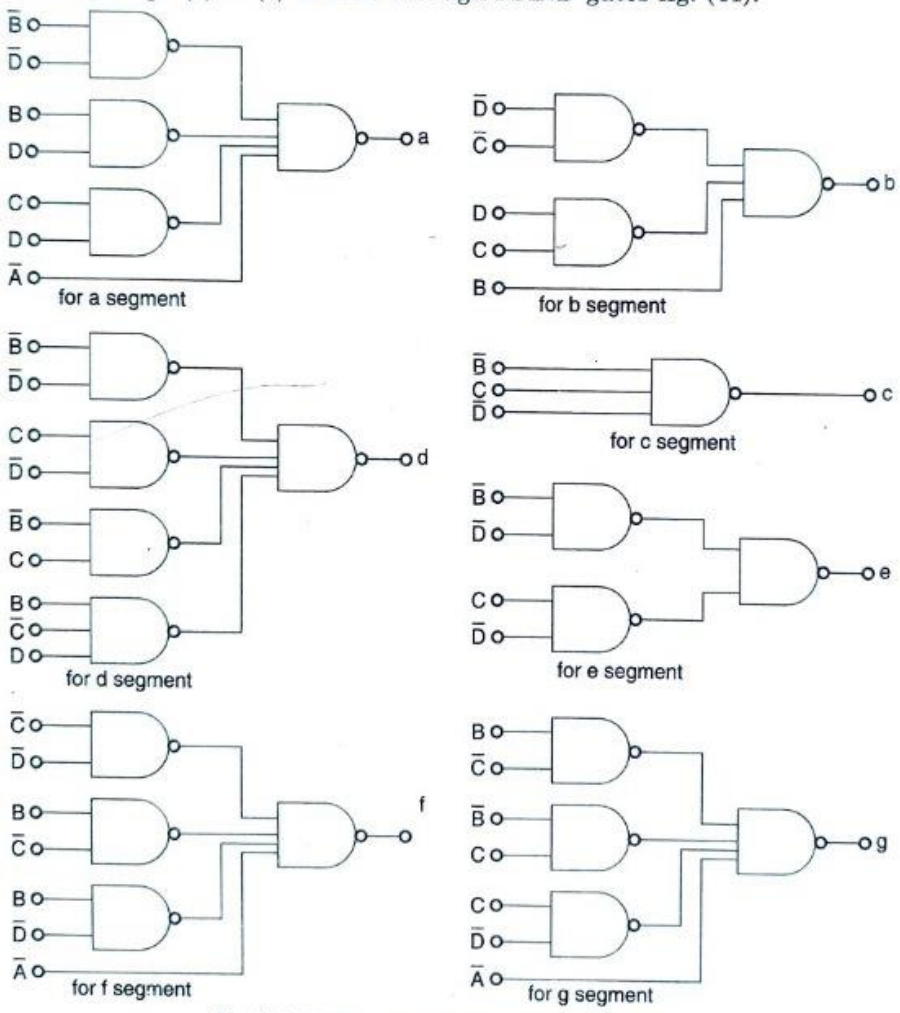


Fig. (41) NAND gate realisation of Eqs. (1) to (7).

We see from the realisations of fig. (41) that a term with single literal must be inverted and then applied to the second level NAND gate. For example, A in eq. (1), $\overline{B}$ in eq. (2) etc. They are inverted and applied as $\overline{A}$ and B as shown.

18.15 MULTIPLEXER (DATA SELECTOR)

A single transmission line can be used to carry several digital signals provided no two signals are sent exactly at the same time. Instead, line is used in short intervals at prescribed times by *each* signal. The circuitry which selects one of several signals at the transmitting end is referred to as a *multiplexer*. At the receiving end, a *demultiplexer* places the received signal on one of several output lines, Multiplexer and de-multiplexer must be coordinated to change in the same time for correct transmission which requires that one or more control lines must be provided in addition to the transmission line. We shall describe a digital multiplexer which will select one of several binary digital signals for transmission over a single line.

Consider the design of a two line-to-one line multiplexer, represented in fig. (46a). The operation is to allow a signal present on the selected line to pass to the output, while the unselected line is ignored.

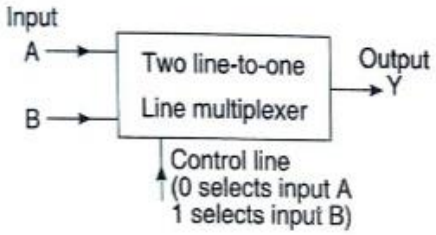
Let C represent control line, A and B the inputs, and Y the output, then equation to describe the desired operation is

$$Y = \overline{C}\ A + CB$$

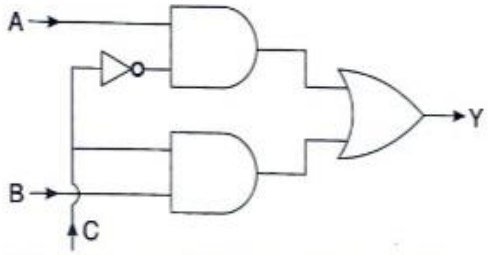
(i) if $C = 0$ then $CB = 0$ and $\overline{C}A = A$ so that input A is selected.

(ii) if $C = 1$ then $CB = B$ and $\overline{C}A = 0$ so that input B is selected.

We note that only *one* input is selected at a time with the help of control line. Logic circuit of fig. (46a) is given in fig. (46b).



(a) Two line to one line multiplexer



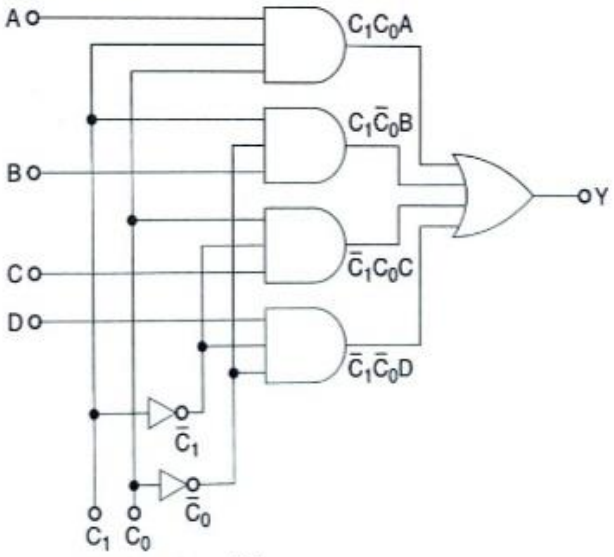
(b) Logic circuit of two line to one line multiplexer

Fig. (46) Selection of one input out of many inputs (output-one, input-many).

Following the same basic pattern a 4 : 1 multiplexer (four line-to-one) can be designed. It is shown in fig. (46c) with its truth table.

Truth table

C_1	C_0	Y
0	0	D
0	1	C
1	0	B
1	1	A



19.5 MASTER-SLAVE J-K FLIP FLOP

Two RS flip flops, with feedback of output of second flip flop to input of first flip flop, are used. One is for input while other is for output, clock pulse (CLK) is inverted for second flip flop ($\overline{CLK}$) . Refer to fig. (9a).

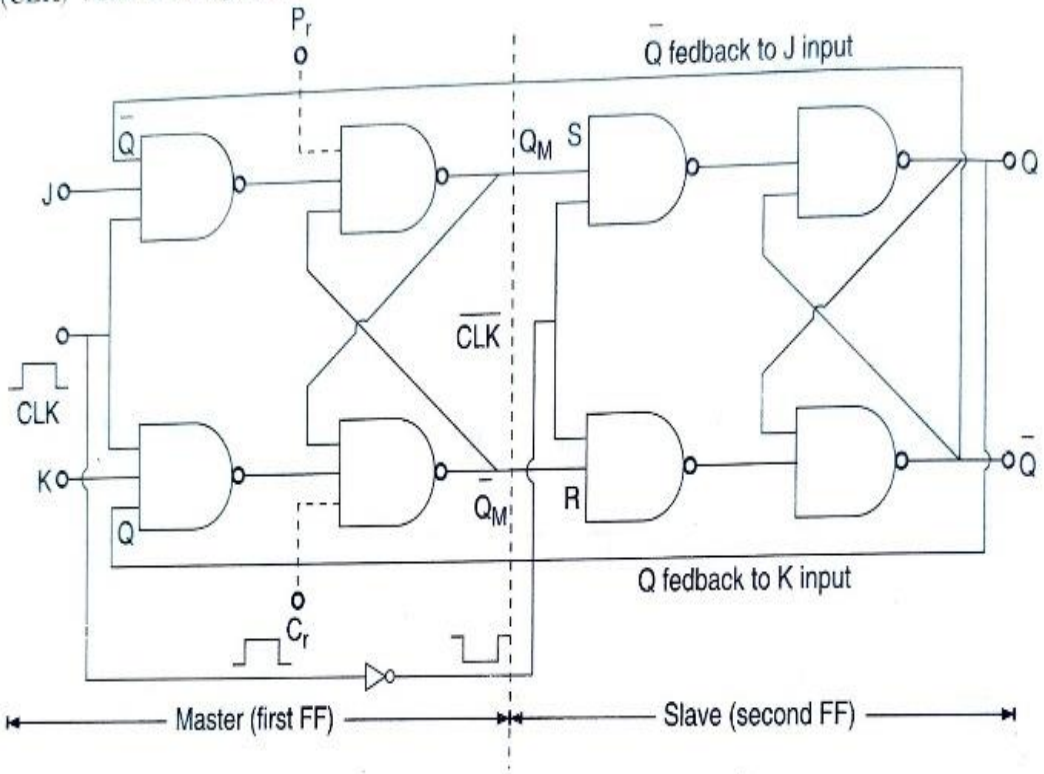


Fig. (9a) J-K master slave flip flop. $S = Q_M$, $R = \bar{Q}_M$.

Case I : When clock pulse is HIGH (CLK = 1, HIGH) : When CLK = 1, first FF operates (enabled) but as $\overline{CLK} = 0$ (LOW) so second FF will not operate (inhibited). Therefore Q, $\bar{Q}$ output of second FF, which are fedback to the input of first FF, can not change so far as CLK remains HIGH. It means that when Q, $\bar{Q}$ do not change and $J = K = 1$, then inputs do not change so that outputs Q_M and Q'_M $(= \bar{Q}_M)$ of first FF are definite (1 and 0, or 0 and 1) and not oscillating. Race around condition is therefore avoided.

Case II : When clock pulse is LOW (CLK = 0) : First FF will not operate but as $\overline{CLK} = 1$, HIGH, the second FF will operate.

Outputs of first FF, Q_M and $\bar{Q}_M$ are inputs to second FF. Consequently outputs Q, $\bar{Q}$ of second FF follow the outputs Q_M, $\bar{Q}_M$ of first FF. In otherwords, second FF simply follows

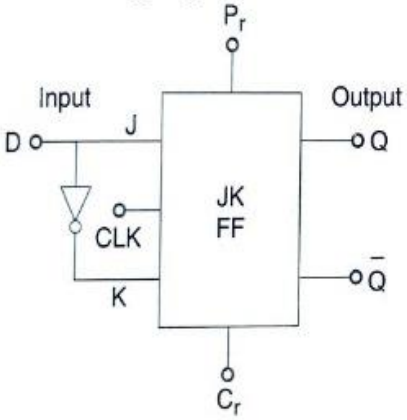
the first FF. Hence first FF is referred to as Master and second FF as slave. Since slave is a RS flip flop, its operation follows the truth table of RS flip flop, mentioned earlier.

(i) If $S = Q_M = 1$ and $R = Q_M = 0$
then $Q = 1$ and $Q = 0$

(ii) If $S = Q_M = 1$ and $R = \overline{Q}_M = 0$
then $Q = 0$ and $\overline{Q} = 1$

Thus in the interval between clock pulses, the value of Q_M is transferred to the output Q (or $\overline{Q}_M$ transferred as $\overline{Q}$). Erratic behaviour does not occur during clock pulse because the cross connected feedback is from the output of the slave to the input of master. *Since the outputs Q and $\overline{Q}$ do not change during the clock pulse, no oscillations can take place.* Thus any possibility of arbitrary output when clock pulse ends is removed.

The D-type Flip-Flop : In this type of flip flop, there is no possibility of ambiguous state. This is achieved by providing JK flip flop with an inverter on one of the input lines. Its symbol and truth a table is shown in fig. (9b). In it we use only middle two rows of truth table of *J-K* flip flop.



J	K	Q_{n+1}
1	0	1
0	1	0

Truth table

Input $D_n = J$	Output Q_{n+1}
0	0
1	1

Fig. (9b)

From truth table it is clear that input is transferred to the output at the end of the clock pulse. Thus *output after CLK, equals the input at D before CLK.* Thus transfer of data from input to output is delayed. It is called delayed FF. The data is as such transferred; terminal *D* is also called as *data input.*

As the bit on *D* line is transferred to the output at the next clock pulse, this unit functions as a 1-bit delay device and is used as a temporary storage latch.

The edge triggered *D*-type flip flop, discussed above, is easily implemented by adding a single *inverter* to the edge triggered S-R flip flop as shown in Fig. (9c).

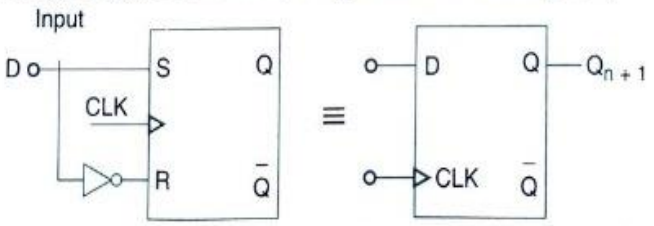


Fig. (9c) An edge triggered S-R flip flop with inverter, acting as a D-flip flop.

Now refer to timing diagram Fig. (9d). We take initially that Q is HIGH. So

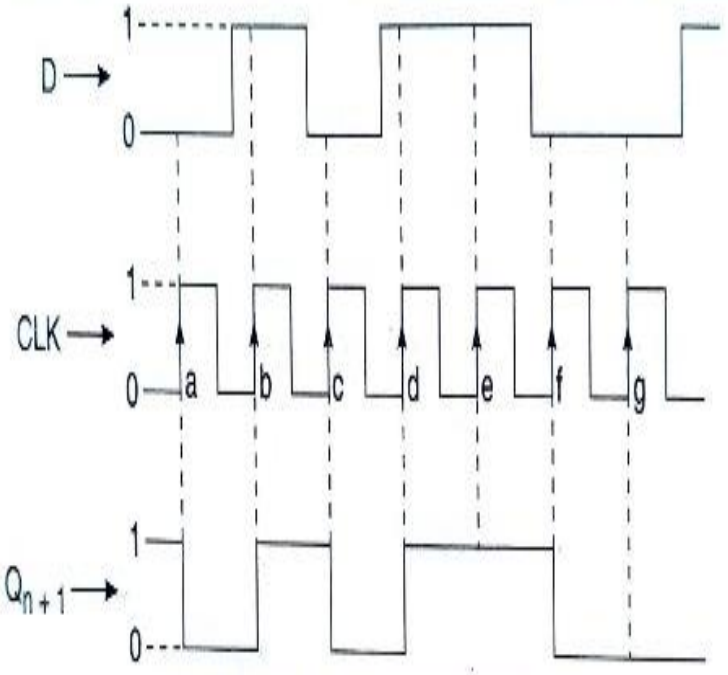


Fig. (9d) Timing diagram of D-type flip flop.

(i) When first PGT occurs at point, *a*, the *D* input is LOW; thus Q_{n+1} will go to the 0 state (LOW).

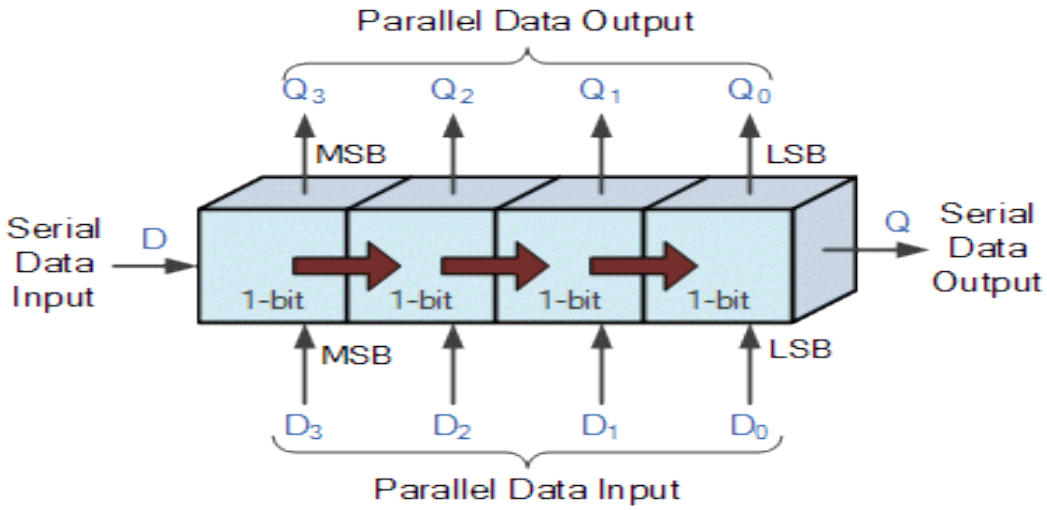
(ii) Between points *a* and *b*, *D* input level changes but it has no effect on Q_{n+1}. Q_{n+1} is storing the LOW which was on *D* at point *a*.

(iii) When PGT at point *b* occurs, Q_{n+1} goes HIGH as D is HIGH at that time. Q_{n+1} stores that HIGH until PGT occurs at point *c* which causes Q_{n+1} to go LOW since *D* is LOW at that time. Thus

If $D = 1$, Q_{n+1} will be 1
If $D = 0$, Q_{n+1} will be 0
} at CLK $0 \rightarrow 1$

The Shift Register

The Shift Register is another type of sequential logic circuit that can be used for the storage or the transfer of binary data. This sequential device loads the data present on its inputs and then moves or "shifts" it to its output once every clock cycle, hence the name **Shift Register**.



A *shift register* basically consists of several single bit "D-Type Data Latches", one for each data bit, either a logic "0" or a "1", connected together in a serial type daisy-chain arrangement so that the output from one data latch becomes the input of the next latch and so on.

Data bits may be fed in or out of a shift register serially, that is one after the other from either the left or the right direction, or all together at the same time in a parallel configuration.

Shift Registers are used for data storage or for the movement of data and are therefore commonly used inside calculators or computers to store data such as two binary numbers before they are added together, or to convert the data from either a serial to parallel or parallel to serial format. The individual data latches that make up a single shift register are all driven by a common clock (Clk) signal making them synchronous devices.

Shift register IC's are generally provided with a *clear* or *reset* connection so that they can be "SET" or "RESET" as required. Generally, shift registers operate in one of four different modes with the basic movement of data through a shift register being:

- Serial-in to Parallel-out (SIPO) - the register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.

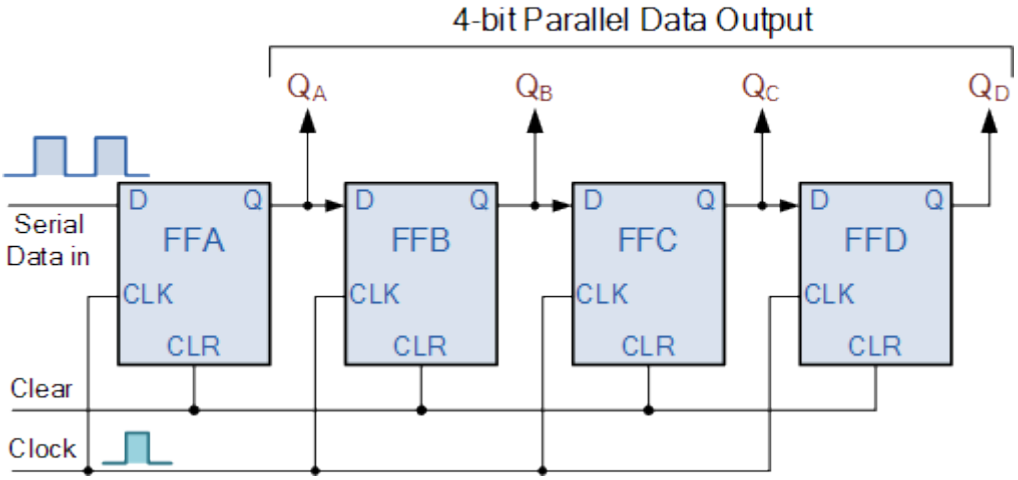
- Serial-in to Serial-out (SISO) - the data is shifted serially “IN” and “OUT” of the register, one bit at a time in either a left or right direction under clock control.
- Parallel-in to Serial-out (PISO) - the parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.
- Parallel-in to Parallel-out (PIPO) - the parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.

Basic Data Movement Through A Shift Register

Clock Pulse No	QA	QB	QC	QD
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1
5	0	0	0	0

Serial-in to Parallel-out (SIPO) Shift Register

4-bit Serial-in to Parallel-out Shift Register



The operation is as follows. Lets assume that all the flip-flops (FFA to FFD) have just been RESET (CLEAR input) and that all the outputs Q_A to Q_D are at logic level “0” ie, no parallel data output.

If a logic “1” is connected to the DATA input pin of FFA then on the first clock pulse the output of FFA and therefore the resulting Q_A will be set HIGH to logic “1” with all the other outputs still remaining LOW at logic “0”. Assume now that the DATA input pin of FFA has returned LOW again to logic “0” giving us one data pulse or 0-1-0.

The second clock pulse will change the output of FFA to logic "0" and the output of FFB and Q_B HIGH to logic "1" as its input D has the logic "1" level on it from Q_A. The logic "1" has now moved or been "shifted" one place along the register to the right as it is now at Q_A.

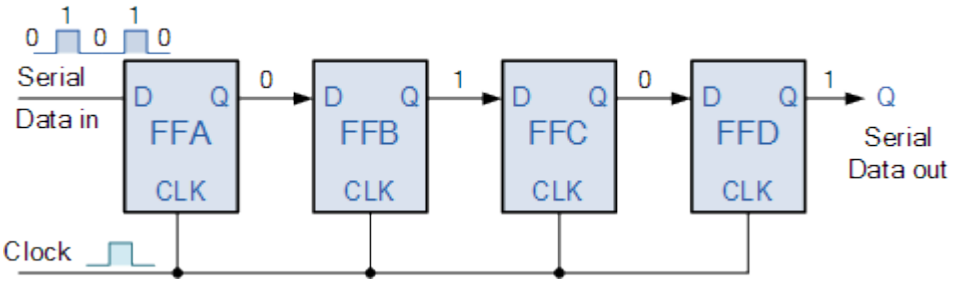
When the third clock pulse arrives this logic "1" value moves to the output of FFC (Q_C) and so on until the arrival of the fifth clock pulse which sets all the outputs Q_A to Q_D back again to logic level "0" because the input to FFA has remained constant at logic level "0".

The effect of each clock pulse is to shift the data contents of each stage one place to the right, and this is shown in the following table until the complete data value of 0-0-0-1 is stored in the register. This data value can now be read directly from the outputs of Q_A to Q_D.

Then the data has been converted from a serial data input signal to a parallel data output. The truth table and following waveforms show the propagation of the logic "1" through the register from left to right as follows.

Serial-in to Serial-out (SISO) Shift Register

This **shift register** is very similar to the SIPO above, except were before the data was read directly in a parallel form from the outputs Q_A to Q_D, this time the data is allowed to flow straight through the register and out of the other end. Since there is only one output, the DATA leaves the shift register one bit at a time in a serial pattern, hence the name **Serial-in to Serial-Out Shift Register** or **SISO**.

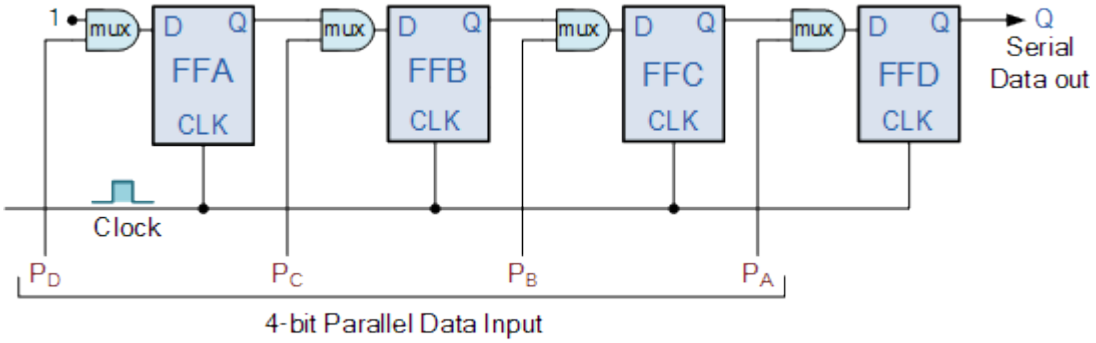


Parallel-in to Serial-out (PISO) Shift Register

The Parallel-in to Serial-out shift register acts in the opposite way to the serial-in to parallel-out one above. The data is loaded into the register in a parallel format in which all the data bits enter their inputs simultaneously, to the parallel input pins P_A to P_D of the register. The data is then read out sequentially in the normal shift-right mode from the register at Q representing the data present at P_A to P_D.

This data is outputted one bit at a time on each clock cycle in a serial format. It is important to note that with this type of data register a clock pulse is not required to parallel load the register as it is already present, but four clock pulses are required to unload the data.

4-bit Parallel-in to Serial-out Shift Register

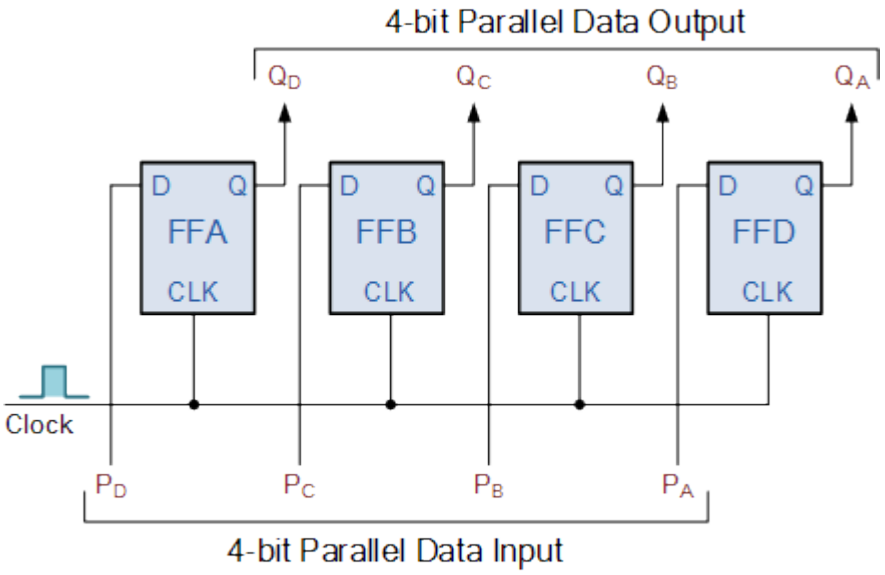


As this type of shift register converts parallel data, such as an 8-bit data word into serial format, it can be used to multiplex many different input lines into a single serial DATA stream which can be sent directly to a computer or transmitted over a communications line. Commonly available IC's include the 74HC166 8-bit Parallel-in/Serial-out Shift Registers.

Parallel-in to Parallel-out (PIPO) Shift Register

The final mode of operation is the Parallel-in to Parallel-out Shift Register. This type of shift register also acts as a temporary storage device or as a time delay device similar to the SISO configuration above. The data is presented in a parallel format to the parallel input pins P_A to P_D and then transferred together directly to their respective output pins Q_A to Q_D by the same clock pulse. Then one clock pulse loads and unloads the register. This arrangement for parallel loading and unloading is shown below.

4-bit Parallel-in to Parallel-out Shift Register



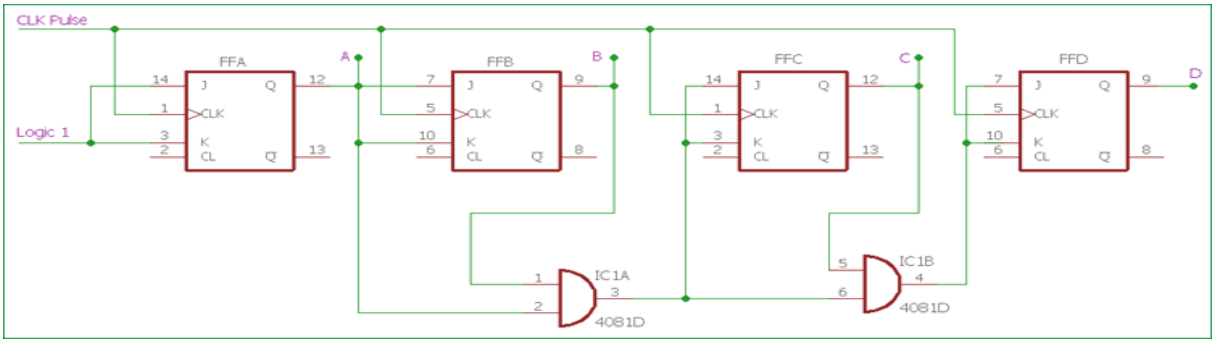
The PIPO shift register is the simplest of the four configurations as it has only three connections, the parallel input (PI) which determines what enters the flip-flop, the parallel output (PO) and the sequencing clock signal (Clk).

Synchronous Counter

Synchrounous generally refers to something which is cordinated with others based on time. Synchronous signals occur at same clock rate and all the clocks follow the same reference clock.

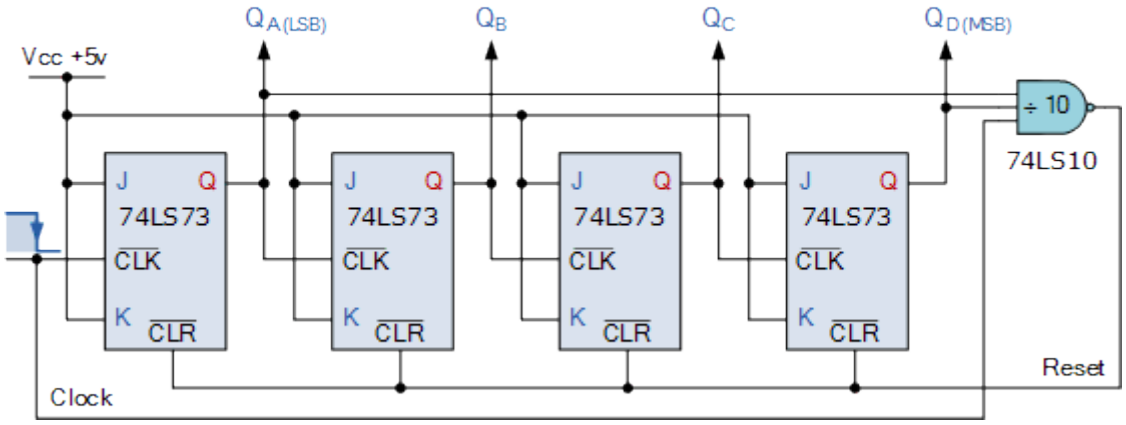
In previous tutorial of Asynchronous Counter, we have seen that the output of that counter is directly connected to the input of next subsequent counter and making a chain system, and due to this chain system propagation delay appears during counting stage and create counting delays. **In synchronous counter**, the clock input across all the flip-flops use the same source and create the same clock signal at the same time. So, a counter which is using the same clock signal from the same source at the same time is called **Synchronous counter**.

Synchronous Up Counter



In the above image, the basic Synchronous counter design is shown which is **Synchronous up counter**. A **4-bit Synchronous up counter** start to count from 0 (0000 in binary) and increment or count upwards to 15 (1111 in binary) and then start new counting cycle by getting reset. Its operating frequency is much higher than the same range Asynchronous counter. Also, there is **no propagation delay** in the synchronous counter just because all flip-flops or counter stage is in parallel clock source and the clock triggers all counters at the same time.

Asynchronous Decade Counter



This type of asynchronous counter counts upwards on each trailing edge of the input clock signal starting from 0000 until it reaches an output 1001 (decimal 9). Both outputs QA and QD are now equal to logic “1”. On the application of the next clock pulse, the output from the 74LS10 NAND gate changes state from logic “1” to a logic “0” level.

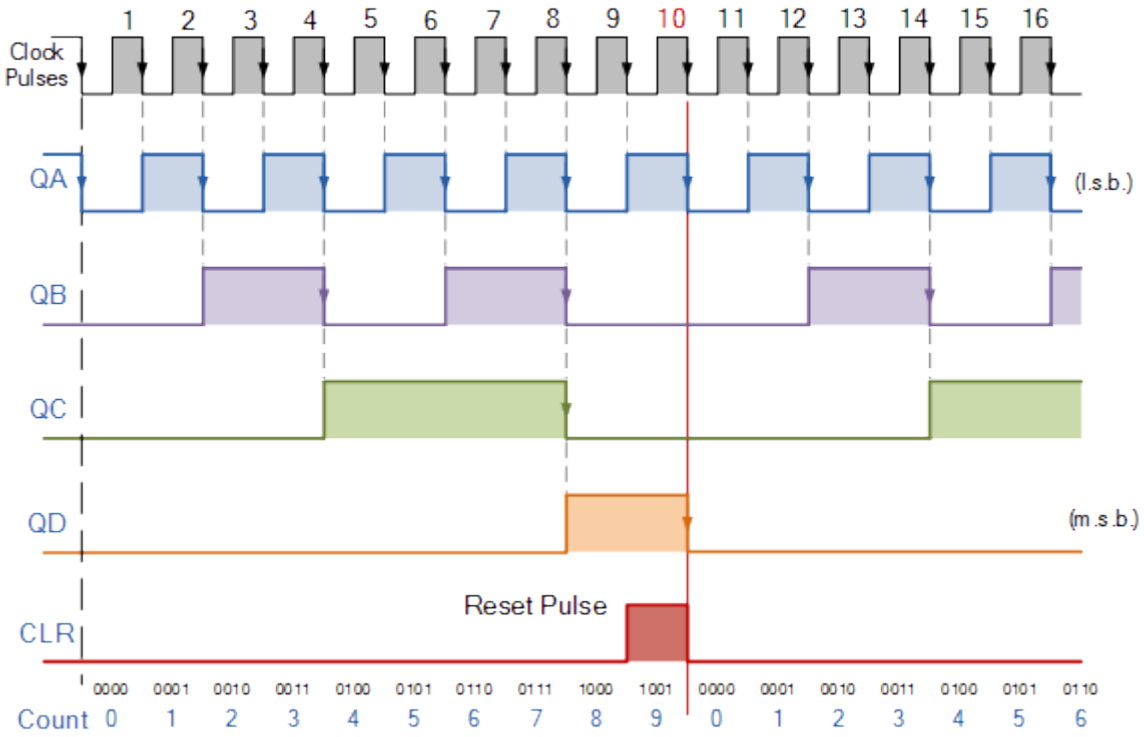
As the output of the NAND gate is connected to the CLEAR (CLR) inputs of all the 74LS73 J-K Flip-flops, this signal causes all of the Q outputs to be reset back to binary 0000 on the count of 10. As outputs QA and QD are now both equal to logic “0” as the flip-flop’s have just been reset, the output of the NAND gate returns back to a logic level “1” and the counter restarts again from 0000. We now have a decade or Modulo-10 up-counter.

Decade Counter Truth Table

Clock Count	Output bit Pattern				Decimal Value
	QD	QC	QB	QA	
1	0	0	0	0	0
2	0	0	0	1	1

3	0	0	1	0	2
4	0	0	1	1	3
5	0	1	0	0	4
6	0	1	0	1	5
7	0	1	1	0	6
8	0	1	1	1	7
9	1	0	0	0	8
10	1	0	0	1	9
11	Counter Resets its Outputs back to Zero				

Decade Counter Timing Diagram



The difference between a synchronous counter and an asynchronous counter

Synchronous Counters	**Asynchronous Counters**
All flip-flops are given the same clock simultaneously	The flip-flops are not given the same clock
There is no connection between the output of a flip-flop and the clock input of the next flip-flop.	The output of a flip-flop is given as the clock input to the next flip-flop
The settling time is equal to the time it takes for the last flip-flop to get activated. This is quite less compared to the asynchronous counters.	The settling time or the time taken for all the flip-flops to get activated is equal to the sum of all the times needed to activate the last flip-flop.
It is known as a *parallel counter*	It is known as a *serial counter*
This design gets more complicated as the number of flip-flops increases	The design of asynchronous counters is easy
Synchronous counters are faster	Asynchronous counters are slower

Counters

A counter is the most versatile and useful subsystems in the digital system. A counter driven by a clock can be used to count the number of clock cycles. Since clock pulses occur at known intervals, the counter can be used as an instrument for measuring time and therefore period and frequency. There are two types of counters: synchronous and asynchronous.

All processors contain a program counter, or PC. – Programs consist of a list of instructions that are to be executed one after another (for the most part). – The PC keeps track of the instruction currently being executed. – The PC increments once on each clock cycle, and the next program instruction is then executed. Counters could be serial or parallel counters or combination of both. Counters could be asynchronous or synchronous counters.

Counters operate in – Count up mode –Count down mode

When counters are cleared, then all the flip flops are 'cleared' and they contain zero. Counter are preset such that the contents of the flip flop represent any desired binary number. A decade counter counts ten events or till the number 10 and then resets to zero. Remember that reset pin we used in all of our counters above. Now it's going to come in handy. In fact, using the logic we use to design the *decade counter*, you can design a counter that can count to any desired number that you wish.

A count till ten won't be possible in a 3-bit counter. Because 2^3has a maximum count of $2^N - 1 = 7$. A 4-bit counter can count up to 15 though. So let's use that. Also, we know that the binary number 1010 represents 10. The four digits are a dead giveaway that we are going to be using four flip-flops.

The reset pins function is to clear the inputs of all the flip-flops. So we need to find a way for this circuit to count up to 10 and then reset to 10. At the count of 10, flip-flops 1 and 3 will be high. Up to 10, this is the first time that this configuration will occur. But remember that we are counting 0 too, so to count ten events, we need to actually count up to 9 and not 10. At the count of 9,

0 – 0000

1 – 0001

2 – 0010

3 – 0011

4 – 0100

5 – 0101

6 – 0110

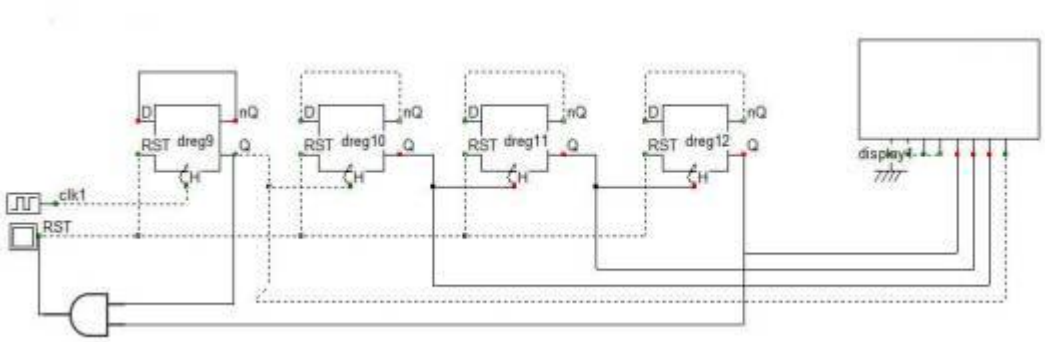
7 – 0111

8 – 1000

9 – 1001

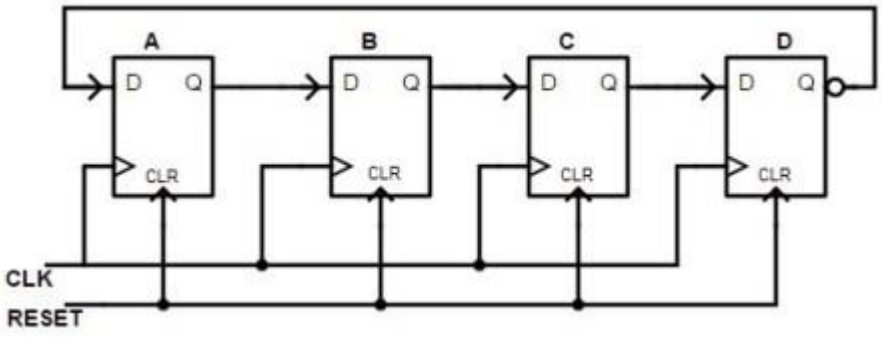
10 – 1010

If we take the outputs from the MSB and LSB flip-flops and connect them to an AND gate, we can get a logic 1 at the count of 9. If we connect the output of this AND gate to the reset pin, then we can reset the flip-flops at the 10th count. This will give us the decade counter.



A ring counter is essentially a slightly modified parallel in serial out (PISO) shift register that acts as a counter. We just take outputs from each of the flip-flops and attach them to a display. Here is a logic circuit of a 4-bit ring counter. It has four flip-flops, and each of them has its own clock input and a reset signal.

Mod n counter has N flip-flops. Where n= 2^N. Just to reiterate, this does not apply here. Mod still has the same meaning, but for ring counters, you cant use the above equation to get the number of flip-flops. Mod means the number of states. As we will see in the working of the ring counter. It has the same number of states as the number of flip-flops in the system. So for *ring counters*, a mod 4 ring counter means it has four flip-flops and four states. States means the number of counts it can have. This will become clearer when we understand the working of this 4-bit ring counter.



4 bit (Mod 4) ring counter (Source)

Since its a Parallel In Serial Shift counter. Let's say we give 1000 as the input. When the first clock pulse appears, the data is loaded to the ring counter. At the second clock pulse, the output of the last flip-flop, 0, gets shifted to the first flip-flop. And the high bit of the first flip-flop moves to the second flip-flop. This continues and repeats itself after every FOUR clock cycles.

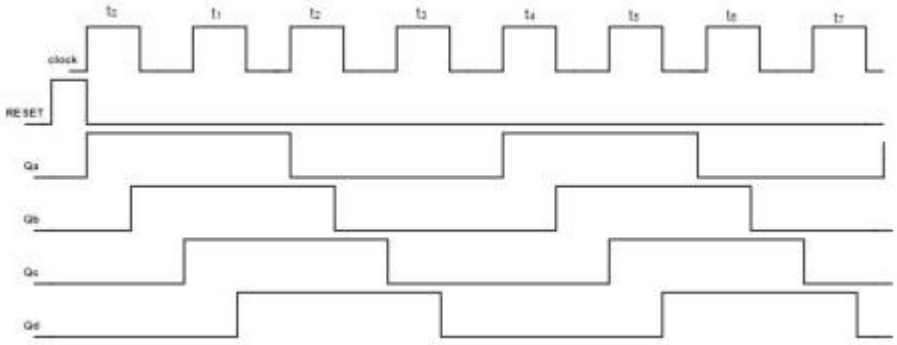
Since it takes the same number of clock cycles as the number of flip-flops in the system, it means that a ring counter has only N states. And hence, in the case of ring counters, the

number of flip-flops is equal to the number of states. Normal binary counters that we saw above had 2^N states.

For example, a 4-bit synchronous up-counter had 16 states. It could count 16 events or from 0-15 decimals. So we are losing a significant number of counts here. Once a number is input to the ring counter, it circulates the same pattern for every n clock cycles. n is the number of flip-flops connected to it.

Hence, it has a frequency of 1/n and is also known as a divide-by-n counter. Check out the pulse diagram and the truth table below to get a clearer picture of the working.

The timing diagram of a 4-bit ring counter



Notice the repeating pattern after the t3 pulse. The 4-bit ring counter repeats itself after four states/pulses/counts. (Source)

19.7 ASYNCHRONOUS (RIPPLE) COUNTERS

A counter can be described as a tallying device that tallies, or counts some number of events. An electronic counter needs that the data be converted into electric pulses, each of which represents one bit of information, or one *happening*. These pulses are introduced at the input and the counter tallies each and every one keeping a cumulative total. So a circuit used for counting the pulses is known as a counter.

There are two types of counters :

(1) Asynchronous counter (ripple counter), and

(2) Synchronous counter

In case of an asynchronous counter, all the flip-flops are *not clocked simultaneously*. That is, all the flip-flops do *not* change states in exact synchronism with the clock pulses : only first FF to which clock pulses are applied responds to clock pulses but the next flip-flop will change states only when its preceding flip-flop has changed its states. That is, output of

one flip-flop drives another. That is how clock pulse effectively ripples through the chain of flip-flops. This type of counter is called ripple counter.

In case of a synchronous counter *all the the flip-flops are clocked simultaneously.*

Counters are available in count up, count down and up-down (reversible) forms. All counters that count *upward* from zero are called *up counters* while those which count *downward* from a maximum count to zero are called *down counters.* Down counters are not as widely used as upcounters.

We shall now describe a popular 4-bit binary ripple counter. The description is for an upcounter.

(A) 4-bit, Binary Ripple Counter : When several flip flops are connected together in a certain way, they form a counting chain that is capable of actually counting or tallying the events. Consider four interconnected T-type flip-flops ($J = K = T$) as shown in fig. (13a). The pulses to be counted are applied *only* to the first-flip flop.

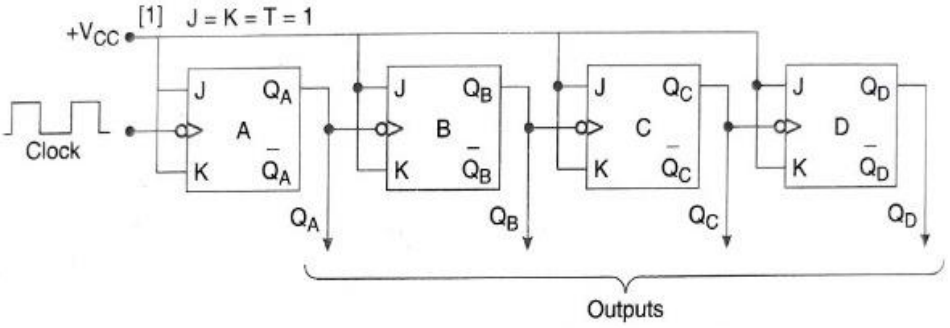


Fig. (13a) Logic diagram : 4 bit binary ripple counter.

For a T-type binary, it may be remembered that :

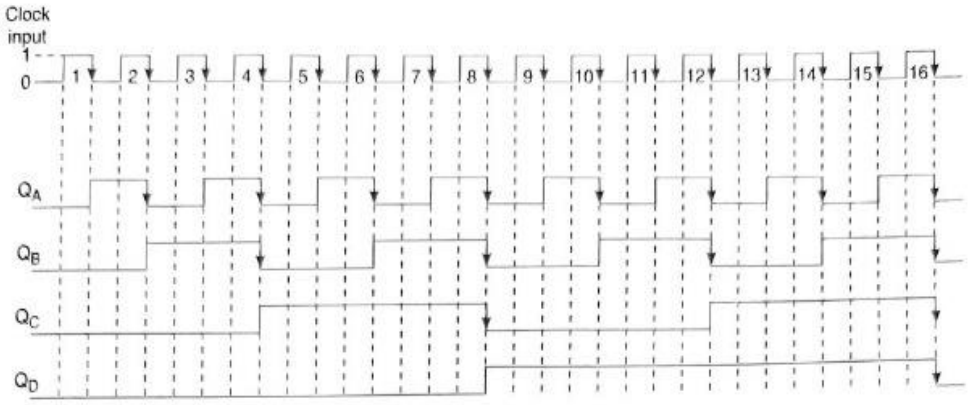
(i) Q_A changes state at the *falling edge of each pulse.*

(ii) All other $Q's$ make a transition *when and only when the output of the preceding flip-flop changes from 1 to 0.*

The output of first flip-flop acts as the trigger input to the next flip-flop and so on. Assume that all flip flip-flops have been cleared by a 1 on all C_D inputs. The function of the chain of flip-flops as to how their states change *i.e.*, their outputs become HIGH (a1) or LOW (a0) can be described as follows, remembering that flip-flops can change their state only at the falling edge of a CP :

(i) *After one CP* (say first *CP*) : After one *CP*, the output of *A* goes HIGH ($Q_A = 1$). It becomes HIGH at the falling edge of first *CP*. The *second flip-flop will not be affected by the positive going edge of the first CP.*

(ii) *When second, fourth and eighth CP arrives* : At the falling edge of second *CP*, first flip-flop, *A*, again changes its state so that $Q_A = 0$ (a LOW). Thus we get the falling edge of Q_A at which the second flip-flop *B*, will be triggered and then its output, Q_B, goes HIGH (a1). It will remain in this state until two more *CP* (numbered 3rd and 4th in fig. 13b) occur. This is because falling edge of Q_A will occur only at the arrival of *fourth CP.* At the falling edge of Q_A (the input of flip-flop *B*) second flip-flop changes its state so that $Q_B = 0$, fig. (13b).



(b) Waveforms

Fig. (13b) Waveforms : 4 bit binary ripple counter. The fig. (13c) shows the sequence of binary states that the flip flops follow as clock pulses are applied continuously. A 4-bit binary counter repeats itself for every 2^N (N = number of flip flops) clock pulses. The counter sequences through in a straight binary progression and has sixteen discrete states from 0 to 2^N - 1.

But with $Q_B = 0$, we get the falling edge of Q_B at which the third flip-flop, C will be triggered so that its output $Q_C = 1$. It will remain in this state until the arrival of *eighth CP* because falling edge of Q_B will occur only at the arrival of eighth *CP*. At the falling edge of Q_B , third flip-flop changes its state so that $Q_C = 0$, fig. (13b).

But with $Q_C = 0$, we get the falling edge of Q_C at which the fourth flip-flop D will be triggered so that its output goes HIGH, *i.e.*, $Q_D = 1$. It will remain in this state until the arrival of *sixteenth CP* because falling edge of Q_C will occur only at the arrival of sixteenth *CP*, fig. (13b).

(iii) *Arrival of sixteenth CP* : After 15 clock pulses, all the flip-flop Q outputs are HIGH (a1). Thus when the sixteenth *CP* arrives to reset A, all other flip-flops are reset *i.e.*, outputs Q_A, Q_B, Q_C and Q_D all go LOW (a0). The circuit then starts to count once more. This is called a scale of 16 counter. Fig. (13c) shows the state of the flip-flops at each count.

Input pulse	Flip flop outputs			
	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16	0	0	0	0

For CP = 13, $Q_A = 1$, $Q_B = 0$, $Q_C = 1$, $Q_D = 1$

All flip flop outputs go high after CP = 15

When CP = 16 arrives to reset A, all the others are also reset because of falling outputs.

Fig. (13c) Table showing state of flip-flops at each count.

Other Uses of this Circuit :

(i) *To decode a count of 13* : Refer to the table fig. (13c). At count 13, $Q_A = 1, Q_B = 0, Q_C = 1, Q_D = 1$. Therefore to get a count of 13, we use a four input AND gate with Q_A , $\overline{Q}_B$, Q_C and Q_D as input. All inputs are a1, *i.e*, $Q_A = 1, Q_B = 1, Q_C = 1, Q_D = 1$, so that $\overline{Q}_B = 0$. Thus we apply 1101 at the input of AND gate and get a count of 13. We note that most significant bit (MSB) is Q_D while least significant bit (LSB) is Q_A.

(ii) *As frequency divider* : From fig. (13b), it is clear that the frequency of output from A is one half that of CP and the frequency of output from B is one-quarter that of CP. It leads to the way of designing 'divide by—' counters, *e.g.*, 'divide by 60' etc.

(iii) *MOD-Number or Modulus* : The counter in fig. (13a) has 16 distinctly different states. Thus it is a *MOD-16 ripple counter*. The MOD-number (or the Modulus) of a counter is the total number of states which the counter goes through in each complete cycle.

$$\text{MOD number} = 2^N$$

where N is number of flip-flops.

The maximum binary number which the counter can reach is equal to $2^N - 1$. Thus a 4-flip-flop counter can count as high as

$$(1111)_2 = 2^4 - 1 = 15_{10}.$$

(B) BCD Decade Counter : A binary coded decimal (BCD) counter is shown in fig. (14). The counter will reset itself to zero after a count of 10. Forced feedback is used to return the counter to reset state after nine natural binary counts. On count 10, all the outputs are LOW, *i.e.* outputs of all flip-flops are a 0. Truth table for this counter is thus same as for a scale of 16 counter upto and including count 9.

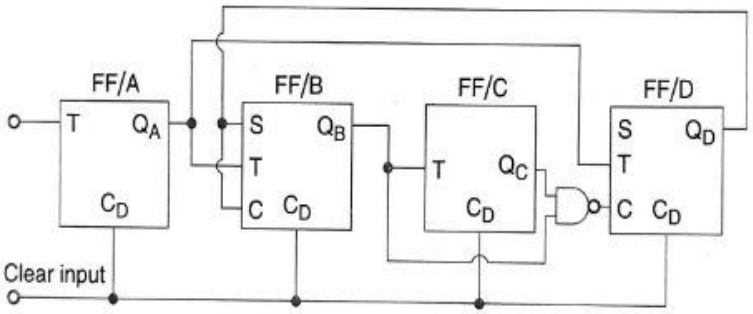


Fig. (14) BCD decade counter.

The operation can be briefed with the help of truth table fig. (13c) as follows :

(i) At the falling edge of every CP, flip-flop A changes its state *i.e.* from a1 to a0, and *vice versa.*

(ii) Flip-flop C changes its state everytime B changes from a1 to a0, *i.e.*, at the falling edge of Q_B fig. (13b). Thus triggering of flip-flop C depends upon the output of B.

(iii) Flip-flop B changes its state when Q_A goes from a1 to a0 (*i.e.*, at the falling edge of Q_A, fig. (13b), *except* on tenth pulse. From fig. (13b), we note that though at falling edge of tenth pulse, Q_A goes from a1 to a0 but Q_B will not rise from a0 to a1. The reason is that because now Q_D has also become a1 and as it is fedback to the input of B, the input of B remains HIGH (a1) and thus its output Q_B cannot change its state, *i.e.*, it continues to be a LOW (a0). In otherwords B, *is inhibited from changing back to a1 at this time.*

Thus at the arrival of tenth pulse, Q_A goes from a1 to a0, Q_B is forced to 0, and $Q_C = 0$ (already LOW). Since $Q_B = 0, Q_C = 0$, there will be a1 at the clear input, C, of the flip-flop D so that Q_D will also be a0. Thus Q output of all flip-flops go to a0 *i.e.*, counter resets to zero, to be ready for next count.

It remained to explain when Q_D goes a 1. We observe from the truth table that flip-flop D never changes its state during counts 1 through 7. This is because at its clear input, C, a sustained 1 is always present on account of either Q_B or Q_C (or both) being 0 when Q_A drops from 1 to 0. Thus input of D remains HIGH and $Q_D = 0$. But *after count 7, this high clear input is removed and* Q_D *goes high (a 1) when* Q_A *goes from 1 to 0. This happens at eighth pulse. The result is that at the tenth pulse FF/B is inhibited and counter resets itself.* It may be remembered that such a reset condition is achieved only after the application of 16th pulse in a scale of 16 counter.

19.8 SYNCHRONOUS COUNTERS

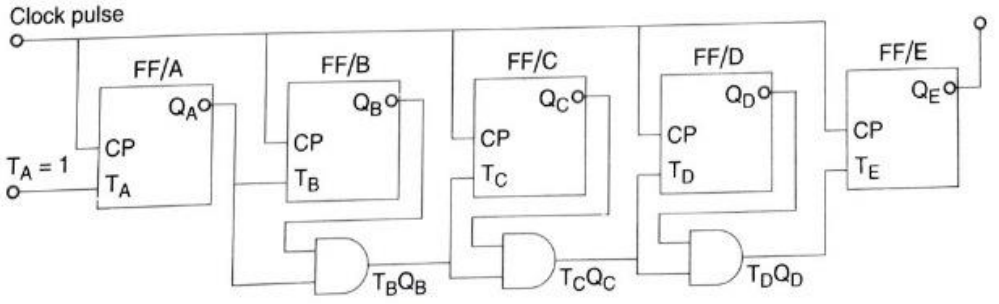
In 4-bit ripple counter in fig. (13b), refer to the input after the seventh pulse. Outputs Q_A, Q_B and Q_C are high. When eighth input pulse is applied, Q_A goes from high to low. This causes Q_B to go from high to low, which causes Q_C to go from high to low. Thus falling edge of eighth pulse causes a transition in each of the succeeding flip-flops, the *effect rippling through the counter.* Thus clock pulse effectively ripples through the chain of flip flops. It causes carry propagation delay (which is the time for a counter to complete its response to an input pulse) *because any flip-flop will not respond unless the preceding flip-flop has completed its transition.* Therefore, when the output of one flip-flop drives another, the counter is called a ripple counter; *FF/ A* has to change states before it can trigger the *FF/ B* flip-flop. *FF/ B* has to change before it can trigger *FF/ C* and so forth. The triggers move through the flip-flops like a ripple in water. Because of this, *the overall propagation delay time* (t_p) *is the sum of the individual delays.* If each flip flop in a 4-bit binary counter has a t_p of 10 ns, the overall propagation delay will be equal to 40 ns. Propagation delay time can be reduced considerably in synchronous counter in which all flip flops are controlled by a *common clock.* There are two methods of flip flops control in synchronous counters :

(i) with ripple (or series) carry, and

(ii) with parallel carry (or carry look ahead).

The latter is the faster of the two methods.

(A) 5-Bit Synchronous Counter with Series Carry : Refer to fig. (15a). Each flip flop is a T-type. The connections to be made to T-inputs are deduced from waveform chart of Fig. (15b). The state of *FF/ A* will change with each pulse, *i.e.*, flip flop toggles from one state to another at each clock pulse. Thus



(a) A 5-bit synchronous counter with series carry (J = K = T)

Fig. (15a) A 5-bit synchronous counter with series carry (*J* = *K* = *T*)

Q_A toggles with each clock pulse, $T_A = 1$ ..... input of A

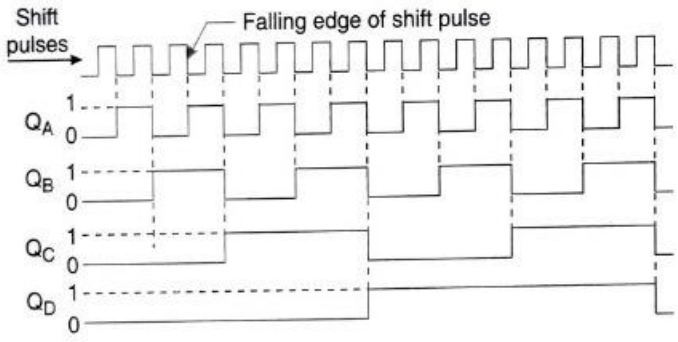
Q_B complements only if $Q_A = 1$, $T_B = Q_A$ ..... input of B

Q_C becomes $\overline{Q}_C$ only if $Q_A = Q_B = 1$, $T_C = Q_A\ Q_B = T_B\ Q_B$ ..... input of C

Q_D toggles only if $Q_A = Q_B = Q_C = 1$, $T_D = Q_A\ Q_B\ Q_C = T_C\ Q_C$ ..... input of D

Q_E toggles only if $Q_A = Q_B = Q_C = Q_D = 1$, $T_E = Q_A\ Q_B\ Q_C\ Q_D = T_D\ Q_D$ ..... input of E.

To perform this logic (*e.g.* $Q_C \rightarrow \overline{Q}_C$ if $Q_A = Q_B = 1$) two input AND gates are used fig. (15a). Since the carry passes through all the control gates, this is a synchronous counter with series carry (or ripple carry). In fig. (15c) all 16 states of the counter are shown.



(b) Waveform chart

Input pulse	Flip flop outputs			
	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16	0	0	0	0

States of FF

(c) States of FF

Fig. (15 b & c)

(B) 4-Bit Synchronous Counter with Parallel Carry : In it, toggle input ($T = 1$) to each flip flop comes from an AND gate that has been excited by the outputs from *every preceding flip flop*. In Fig. (16), a 4-bit synchronous counter with parallel carry is shown. We observe that each AND gate to *FF*/ *D* will require three inputs Q_A, Q_B and Q_C. Similarly each AND gate to *FF* | *C* will require two inputs Q_A and Q_B. We note that :

(i) *FF*/ *A* will toggle with each clock pulse. This is achieved by connecting J_A and K_A to a high level ($J_A = K_A = 1$, *i.e.*, $T_A = 1$).

(ii) *FF*/ *B* must change state whenever $Q_A = 1$. This is achieved by connecting J_B and K_B to Q_A.

(iii) *FF*/ *C* changes state only when $Q_A = Q_B = 1$. For achieving it Q_A and Q_B are connected through AND gate to J_C and K_C , as shown in fig. (16).

(iv) *FF*/ *D* changes state only when $Q_A = Q_B = Q_C = 1$. This is achieved by connecting Q_A, Q_B and Q_C through AND gate to J_D and K_D.

Table shown in Fig. (15c) shows all the 16 states of the counter.

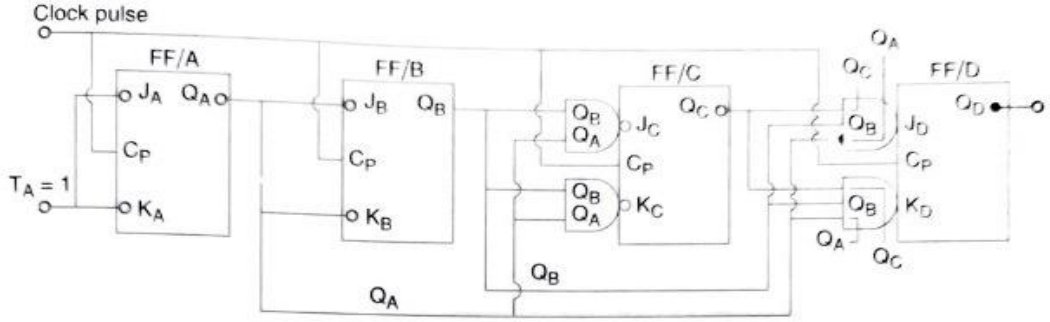


Fig. (16) A 4-bit synchronous parallel counter.

(C) Synchronous Decade Counter with Parallel Carry : The waveform chart is given in fig. (15b) except that after the tenth pulse all waveforms return to a 0 in a decade counter, fig. (17). In fig. (15b) we observe that since $Q_A = 0$ and $Q_C = 0$ after tenth pulse. *FF/ A* and *FF/ C* are excited as in 16 : 1 synchronous counter so that

$$T_A = J_A = K_A = 1$$
$$T_C = J_C = K_C = T_B\ Q_B = Q_A\ Q_B$$

For further flip flops in a decade counter, we require as under :

(i) We note from fig. (15b) that Q_B toggles if $Q_A = 1$. But we do not want that Q_B should go to 1 after tenth pulse. To prevent Q_B from going 1 after the tenth pulse, *it is inhibited by* $\overline{Q}_D$. The reason is that because now Q_D has also become a1, $\overline{Q}_D$ *is a*0 *and is fedback* to the input of AND gate feeding *FF/ B*, so that

$$T_B = Q_A\ \overline{Q}_D = 0$$

Thus as $J_B = K_B = 0$, Q_B will not go a1 *i.e., it is inhibited.*

(ii) We want *FF/ D* to change state from 0 to 1 after eighth pulse for which we need

$$Q_A = Q_B = Q_C = 1$$

so that $J_D = K_D = 1$ giving output $Q_D = 1$. It is done through three input AND gates, fig. (17).

(iii) We want *FF/ D* to return to a state 0 from 1 after tenth pulse. For this we need

$$Q_A = 1,\ Q_B = 0 \text{ and } Q_C = 0$$

so that $J_D = 0$, $K_D = 0$ before tenth pulse, giving $Q_D = 0$.

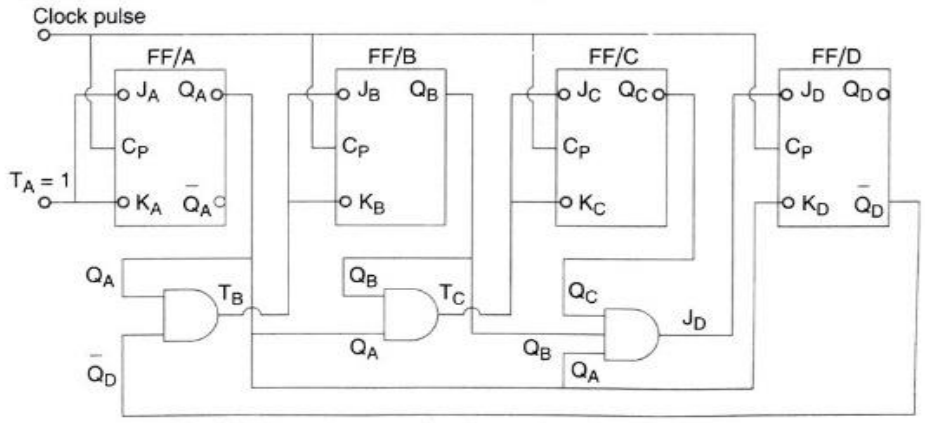


Fig. (17) A synchronous decade counter with parallel carry.

The above three requirements which converts a 16 :1 counter, earlier described, into a decade counter have been implanted through a logic circuit.

UNIT 5

IC Fabrication and IC Timer

An IC is complete electronic circuit in which both active and passive components are fabricated on an extremely tiny single chip of silicon. J.S.Killby was the first to develop (in 1958) an integrated circuit - a single monolithic silicon chip in which active and passive circuit elements were fabricated by successive diffusions and depositions.

Advantages

Following are the advantages offered by integrated circuits :

i. Due to the processing of large quantities of the components , the cost is low .
ii. The size is small.
iii. They have high reliability because all the components are fabricated simultaneously and there are no soldered joints .
iv. To obtain better functional characteristics, more complex integrated circuits may be used and hence the performance is improved .
v. There are no inter-connection errors.
vi. Temperature differences between parts of a circuit are small.
vii. A close matching of components and temperature coefficients is possible because they are fabricated simultaneously by the same processes.

Limitations

Following are the limitations of the integrated circuits :

i. The inductors can not be integrated directly.
ii. Capacitors and resistors are limited in maximum value.
iii. Resistance and capacitance values are often dependent on voltage.
iv. High grade P-N-P unit is not possible easily.
v. Power dissipation is limited.
vi. Low noise and high voltage operation are not easily obtained.
vii. High frequency response is limited by parasitic capacitance.

1. Wafer Preparation

A P-type silicon bar is taken and cut into thin slices called wafers (Fig. 31.5). These wafers after being lapped and polished to mirror finish serve as the base or substrate for hundreds of ICs.

The enlarged views of the circular and rectangular wafers are shown separately in Fig. 31.6.

2. Epitaxial Growth

As shown in Fig. 31.7, an N-type of silicon layer (about 15 μm thick) is now grown on the P-type substrate by placing the wafer in a furnace at 1200°C and introducing a gas containing phosphorus (donor impurity). It is in this epitaxial layer that all active and passive components of an IC are formed. This layer ultimately becomes the collector for transistors or an element for a diode or a capacitor.

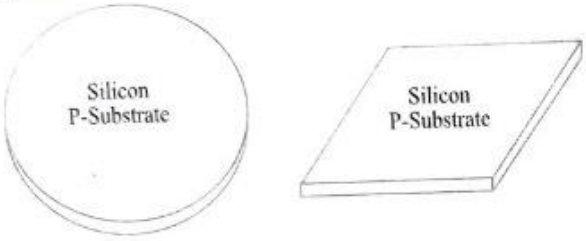


Fig. 31.6

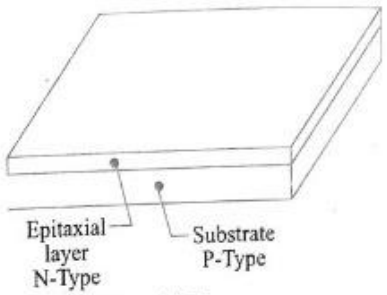


Fig. 31.7

3. Oxidisation

A thin layer of silicon dioxide (SiO_2) is grown over the N-type layer by exposing the wafer to an oxygen atmosphere at about 1000°C (Fig. 31.8).

4. Photolithographic Process

This involves selective etching of SiO_2 layer with the help of photographic mask, photoresist and etching solution [Fig. 31.9 (*a*)]. It helps to select particular areas of the N-layer which are subjected to an isolation diffusion process.

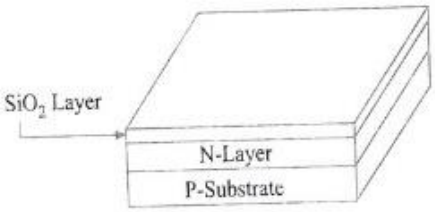


Fig. 31.8

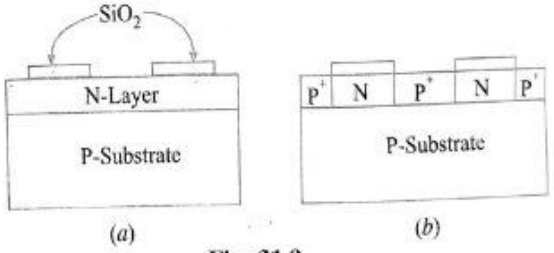
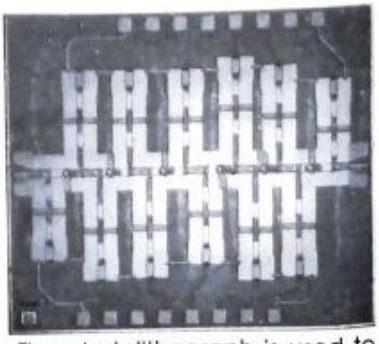


Fig. 31.9

5. Isolation Diffusion

The wafer is next subjected to a P-type diffusion process by which N-type layer is isolated into islands on which transistor or some other component is fabricated [Fig. 31.9 (*b*)]. The heavily-doped regions marked P^+ result in improved isolation between the active and passive components which will be formed in the N-type islands of the epitaxial layer.



The photolithograph is used to add circuit elements to the wafer. The wafer is coated with layer of a chemical called photoresist.

6. Base and Emitter Diffusion

The P-type base of transistor is now diffused into the N-type layer which itself acts as collector. The sequence of steps is the same as in 4 and 5 above *i.e.*, by the use of photoresist and mask which creates windows in the SiO_2 layer as shown in Fig. 31.10. It is carried out in a phosphorus atmosphere. Next, N-type emitter is diffused into the base after another photoresist and mask process as shown in Fig. 31.11. Of course, no further N-type diffusion is required for the resistor which uses the resistivity of the P-type material itself for the purpose.

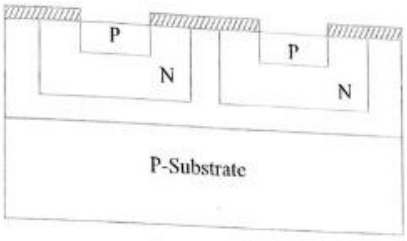


Fig. 31.10

In this way, we have fabricated one NPN transistor and one resistor simultaneously as shown in Fig. 31.11.

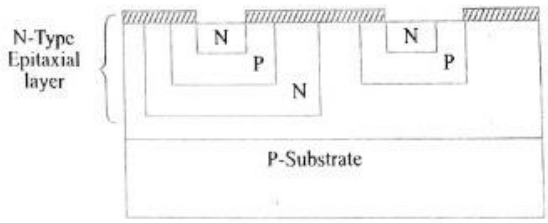


Fig. 31.11

7. Pre-ohmic Etch

For good metal ohmic (non-rectifying) contact with diffused layers, N^+ regions are diffused into the structure as shown in Fig. 31.12. This is done once again by the SiO_2 layer, photoresist and masking process.

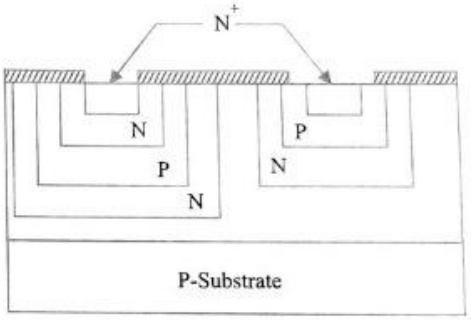
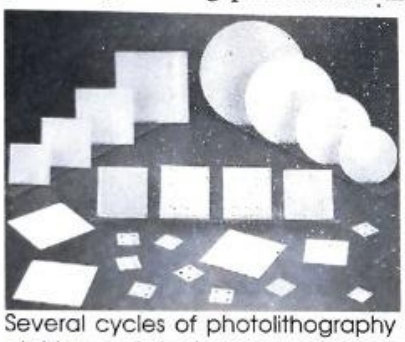


Fig. 31.12

8. Metallization

It is done for making interconnections and providing bonding pads around the circumference of the chip for later connection of wires. It is carried out by evaporating aluminium over the entire surface and then selectively etching away the aluminium to

leave behind the desired inter-connecting conduction pattern and bonding pads. The final circuit alongwith its schematic is shown in Fig. 31.13.



Several cycles of photolithography etching and doping are performed producing multiple layers of circuit elements on the wafer.

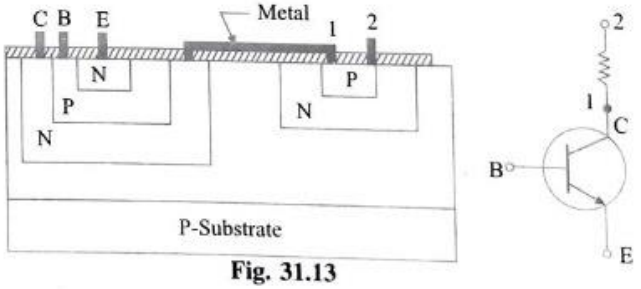


Fig. 31.13

9. Circuit Probing

Each IC on the wafer is checked electrically for proper performance by placing probes on the bonding pads.

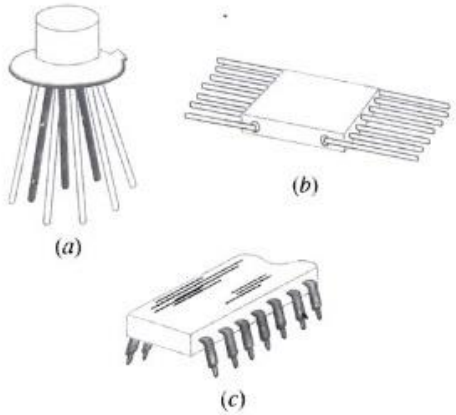


Fig. 31.14

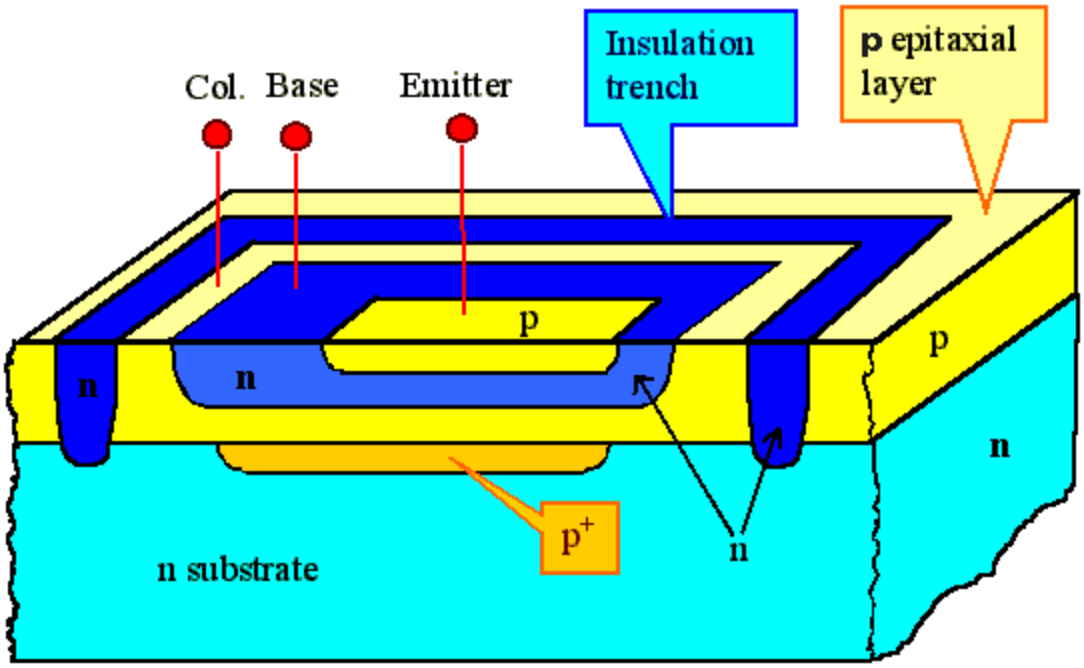
Faulty chips are marked and discarded after the wafer has been scribed and broken down into individual chips.

10. Scribing and Separating into Chips

Once the metallization is complete, wafer is broken down into individual chips containing the integrated circuits. For this purpose, wafers are first scribed with a diamond tipped tool and then separated into single chips.

11. Mounting and Packing

The individual chip is very small and brittle. Hence, it is cemented or soldered to a gold-plated header through which leads have already been connected.



1. Epitaxial growth : The word epitaxial growth is derived from "epi" means upon and "teinein" means arrange. Epitaxial growth is a process or chemical reaction to from a thin film of a single crystal (mono crystalline) silicon (from a gaseous solution or vapour phase)with certain conduction properties on the surface of another silicon wafer or slice. The epitaxial layer may be either P-type or N-type. The basic chemical reaction used to describe the epitaxial growth of pure silicon is the hydrogen reduction of tetrachloride;

$$SiCl_4 + 2H_2 \rightleftharpoons^{1200^{\circ}c} Si + 4HC1$$

As the epitaxial film of specific impurity concentrations is requied and hence it is necessary to introduce impurities such as phosphine (PH_3) for N-type doping or biborane ($B_2 H_6$) for P type doping into silicon tetrachloride . Hydrogen is bubbled through the volatile silicon compound , causing it to vaporize.

Fig shows the diagrammatic representation of a system for production growth of silicon epitaxial layers. The apparatus consists of a long cylindrical quartz tube which is encircled by a radio frequency induction coil. The silicon wafers are placed on a rectangular graphite rad

called a boat . This boat is inserted in the reaction chamber .(i.e,a special type of furnace) where the graphite is heated inductively to about 1200°C. At the input of reaction chamber a control console permits the introduction of various gases required for the growth of appropriate expitaxial layers. Silicon and dopant atoms from the vapour skid about on the surface of the growing epitaxial film until they find a correct position in the lattice structure by inter atomic forces .

The important features of the expitaxial process are as following :

i. The atoms of newly grown layer are arranged in single fashion on the single crystal substrate . Moreover , the lattice structure of the newly grown layer is an exact extension of the substrate crystal structure as shown in fig (8).

ii. The impurity concentration in expitaxial layer may be controlled within wide limits and complex impurity profiles may be grown .

Masking and Etching

In monolithic technique a selective removal of SiO_2 to form openings through which impurities may be diffused is required . For this purpose photolithography is used . This process is shown in fig .(9). The following steps are followed

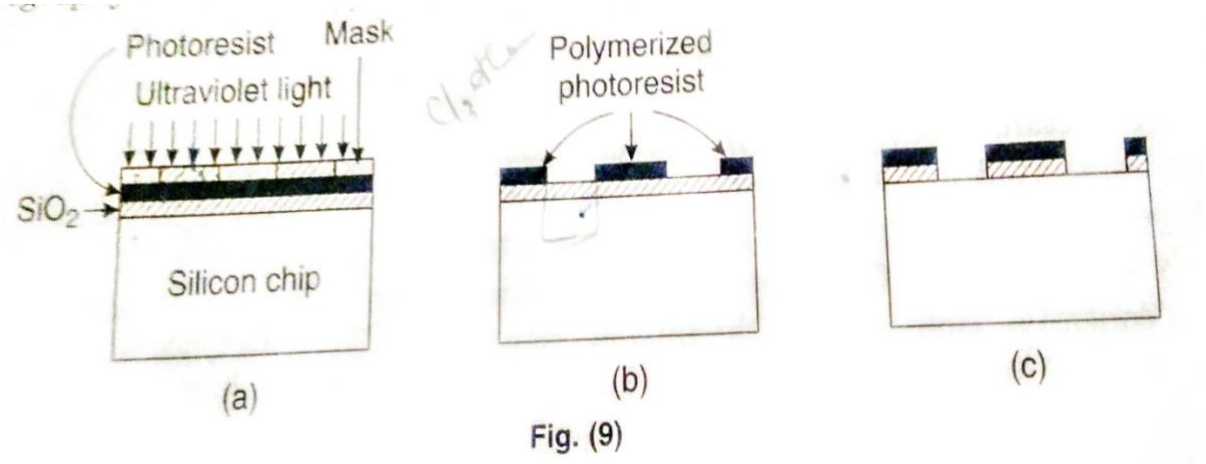


Fig. (9)

i. The wafers is coated with a film of photosensitive emulsion (such as Kodak photoresist KPR).

ii. A large black and white layout of the desired pattern of openings is made and then reduced photographically. This mask (negative or stencil of required dimensions) is placed over the photoresist as shown in fig. Now the photoresist is exposed to ultraviolet light through the mask . Due to ultraviolet light, the photoresist becomes polymerized under transparent regions of the mask .

iii. The mask is removed and the wafer is developed by using a chemical like trichloroethylene. The chemical dissolves the unexposed or un polymerized portion of KPR and leaves the surface patters as shown in fig.

iv. The un removed emulsion is now fixed and becomes resistant to the corrosive etches used next .

v. The chip is immersed in etching solution of hydro-fluoric acid. This removed SiO_2 from the area through which diffusion has to occur . Here it should be noted that the portions of SiO_2 which are protected by photoresist are not affected by the acid after etching .

vi. After diffusion of impurities , the KPR mask is removed with a chemical solvent like hot H_2SO_4 and by means of chemical abrasion process .

Diffusion of Impurities

i. The first step is called deposition . In deposition process the silicon slice is heated in impurity dopant vapour so that a high concentration of dopant atoms is formed on its surface .

ii. The second steps is called diffusion steps. In the diffusion step the dopant deposited silicon slice is removed to another furnace where it is heated to a higher temperature. Now the dopant atoms diffuse into the silicon . The depth of penetration of diffusion and the concentration within the slice depend on time , temperature , the kind of dopant and its original concentration.

When a P-type impurity is diffused into the surface of N-type slice in such a way that the density of P-type atoms exceeds the original density of N-type atoms in slice , the surface will be changed to P-type . A P-N junction is formed a small distance inside from the surface where the density of diffused P-type atom equal to original N-type density . It is also possible to make a second diffusion into a region that has been formed by first diffusion . In the second diffusion

the impurity concentration should be greater than that produced by first diffusion. Again a second PN junction will be formed. The combined result will be N-P-N structure .

Monolithic Integrated Components

Integrated resistors

A resistor can be performed in a silicon wafer by diffusing a suitable impurity into a defined region. This value of the resistor so formed depends upon

i)the concentration of impurity

ii)the dimentions of the region at the surface

iii) the depth to which the impurity is diffused in.

In the fabrication of integrated resistors, P type base diffusion is most commonly used, although N type emitter diffusion may also be employed. Most resistors in integrated circuits are formed at the same time as the P type transistor base region. The diffusion layers are extremely this so that it is more convenient to express the resistivity of the layer interms of what is called as sheet resistance R_s of the layer.

Sheet resistance

Consider the case of a sheet of resistive material of resistivity(ρ), of length and width ω. The resistance of this conductor in ohm/square for the direction of current flow is given by

$$\mathbf{R_s = \rho / y}$$

Where y is the thickness. R_s is independent of the size of the square and depends only on the resistivity of the material and the thickness of the layer. In order to design a resistorof 100 ohm from a material of 10 ohm/square, we merely put 10 squares in succession and make contact to the ends. $R= R_s L/\omega$ length and width of diffused area respectively. Variables available in the design of diffused resistors are i) the strip length L ii) the strip width ω. Strip widths of less than one mil is not mormally used because with ω= 1 mil a line width variation of 0.1 mil due to mask drawing error or due to mask alignment or due to photographic resolution error may result in 10% resistance tolerance error. In practice monolithic base diffusion resistors have values from 20 Ω to 30kΩ. When high values of reistance are required, an alternative to increase the strip length is to reduce the P-type thickness and effective concentration by diffusion into it an N type region at the same time as the transistor emitter diffusion. This method is behaviour more difficult to control than increasing the length of the strip.

THE 555 IC TIMER

The 555 timer is an IC timer device. It can operate both as monostable and astable multivibrator. This monolithic device has advantages over discrete circuits of monostable and astable multivibrator. It has fewer circuit connections and provides improved performance . It generates a pulse whose width can be varied by varying externally connected resistance and capacitance (R and C_T).

Circuit of the 555 timer : It can operate as an astable multivibrator or it can be triggered externally for monostable mode of operation . It has three inputs : THRESHOLD ; TRIGGER and RESET. These inputs control the states of the output terminal and discharge terminal. The output of the flip flop is Q which is also used as an output terminal taken through an output stage. The three equal resistances R establish reference voltage levels $V_1 = 2V_{cc}/ 3$ for comparator - 1 and $V_2 = V_{cc} / 3$ for comparator – 2 . These reference levels are required to control the timing as explained below :

i. **SET state of FF(Flip Flop) :** On a negative transition of pulse applied at the trigger terminal and when the voltage at the trigger terminal passes through $V_{cc} / 3$, the output of the comparator - 2 changes of state sets the flip flop (FF) . The output at the output terminal is high (logic -1 state) .

ii. **RESET state of FF :** when voltage applied at the threshold terminal of comparator-1 goes positive and passes through reference level $2V_{cc} / 3$, the output of comparator – 1 changes state. This changes of state resets the flip flop . The output at the terminal is low (logic – 0 state). A separate reset terminal is provided for the timer and is used to reset the flip flop externally .

Since a high current of order of 200 mA is sourced by the output stage, capacitor, C_T, is connected between discharge terminal and ground. when Q_1 and OFF , the capacitor changes and when Q_1 is ON , it discharge quickly . The top of C_T is also connected to THRESHOLD so that capacitor voltage is applied to threshold input.

A. **Timer as Monostable Multivibrator :**

B.

(i) When no trigger input is applied , capacitor C_T is held in the discharged state. In this case output is low .

(ii) When trigger input is applied and ad the trigger voltage passes through V_{cc} / 3 (threshold levels of comparator- 2), comparator – 2 changes its output state so thst flip flop is sets i.e, $Q^- = 0$ and tansistor Q_1 becomes OFF . Therefore timing cycle begins ,i.e., capacitor C charges up exponentially through R_T, towards V_{cc} with time constant $R_T C_T$, according to

$$\mathbf{V_c = V_{cc} (1-e^{-t/R_T C_T}),}$$

Where V_c is the voltage across the capacitor at any time, t .

(iii) When this voltage V_C, reaches $2\,V_{CC}/3$ (threshold level of comparator-1), as it is connected to threshold terminal, comparator-1 changes its output state so that flip flop is reset, *i.e.*, $\bar{Q} = 1$. This makes the transistor Q_1 ON and the capacitor discharges rapidly to ground; *the timing cycle is completed. Once the circuit is triggered, it is insensitive to further triggering pulses until the timing cycle is completed.*

(iv) From points (ii) and (iii), we note that time period of the timing cycle is the time required for the capacitor to charge from zero to $2\,V_{CC}/3$. This period can be obtained on putting $V_C = 2\,V_{CC}/3$ at $t = T$ in eq. (1). That is

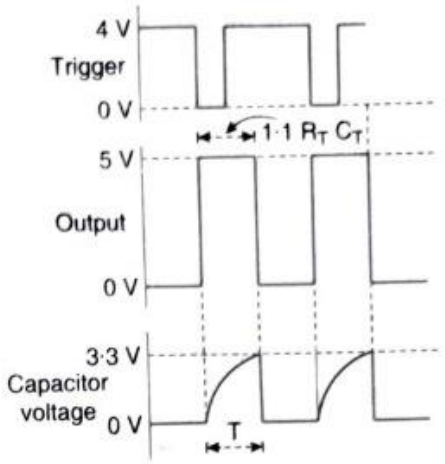


Fig. (77) 555 timer, used as a one shot multivibrator. Note $V_c = 2\frac{V_{cc}}{3} = 2 \times \frac{5}{3} = 3{\cdot}3\ V$

$$2\,V_{CC}/3 = V_{CC}\,(1 - e^{-T/R_T C_T})$$

$$T = R_T\,C_T\,\log_e \frac{V_{CC}}{V_{CC} - \frac{2}{3}V_{CC}} \cong 1{\cdot}1\,R_T\,C_T \qquad \ldots(2)$$

Thus pulse width is determined by external resistance and capacitance.

(B) *Timer used as Astable Multivibrator* :

External connections for astable operation are shown in fig. (78). In this operatio circuit does not require any external trigger signal; therefore, trigger terminal is connecteu to threshold terminal so that *at all time, V_C, is applied to both these inputs.* Further two series resistors R_A and R_B are also used, whose common junction is connected to discharge terminal. Its operation is as follows :

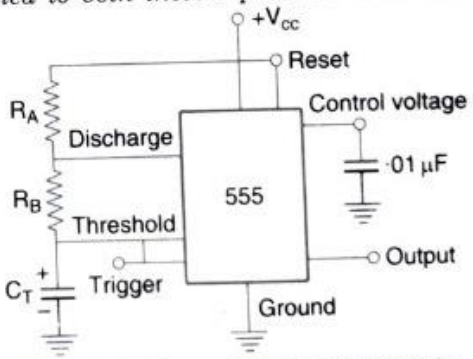


Fig. (78) 555 timer : External connection for astable operation.

Operation : During charging up period transistor Q_1 is held open by the flip-flop and capacitor charges through series connected resistors R_A and R_B. When voltage across capacitor reaches $2\,V_{CC}/3$ (reference level of comparator-1) comparator-1 changes its output state and it changes the state of flip-flop so that transistor Q_1 is now ON. The capacitor then discharges through R_B until its voltage drops to $V_{CC}/3$ (reference level of comparator-2). This comparator then changes the state of flip-flop again which in turn makes the transistor Q_1 OFF and thus the cycle repeats itself.

Charging period : As is clear from above description, charging of the capacitor (through R_A and R_B) starts from $V_{CC}/3$ (and not from zero as in case of monostable operation) and continues upto $2\,V_{CC}/3$. Therefore eq. (2) for this case becomes :

Charging period : $T_1 = C(R_A + R_B)\log_e \dfrac{V_{CC} - V_{CC}/3}{V_{CC} - 2V_{CC}/3}$

$= C(R_A + R_B)\log_e 2 = 0{\cdot}7(R_A + R_B)C$

Discharge period : Capacitor discharges (through R_B only) from $2V_{CC}/3$ towards zero volt. This discharge is terminated at $V_{CC}/3$ at which comparator-2 changes state. Hence discharge period is determined by the equation

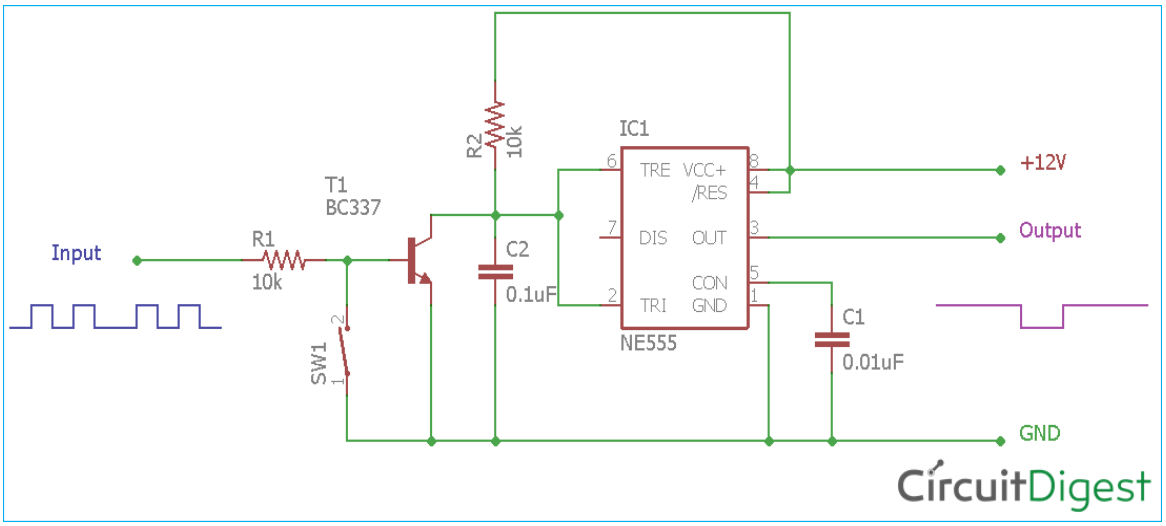
$$T_2 = C R_B \log_e \frac{0 - 2V_{CC}/3}{0 - V_{CC}/3} = 0{\cdot}7 R_B C.$$

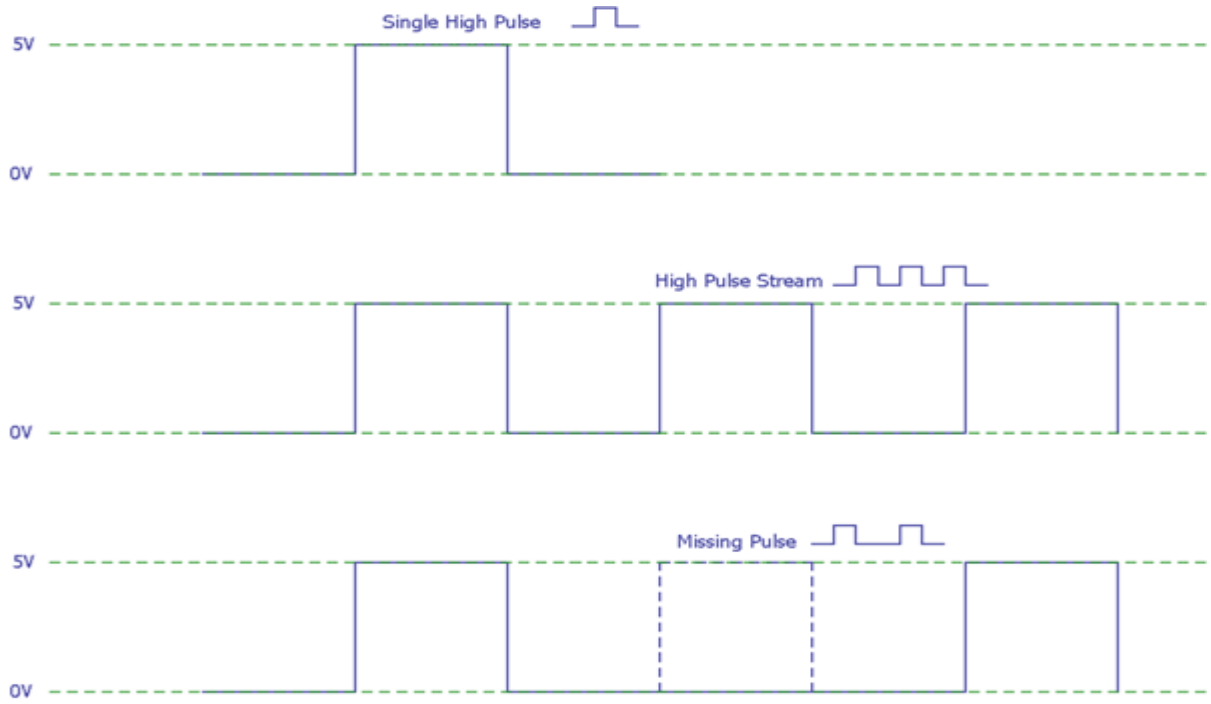
Total period : $T = T_1 + T_2 = 0{\cdot}7(R_A + 2R_B)C.$

Charging and discharging intervals differ by $0{\cdot}7 R_A C.$

MISSING PULSE DETECTOR

Whenever the trigger pulse is low, the emitter diode of the transistor Q is forward biased. The capacitor C gets clamped to few tenths of a volt (0.7v). The output of the timer goes HIGH. The circuit is designed show that the time period of the monostable circuit is slightly greater(1/3 longer) than that of the triggering pulses. So long the trigger pulse train keeps coming at pin, that output remain HIGH. However, if a pulse misses, that trigger input is high and transistor Q is cut off. The 555 timer enter into normal state of monostable operation. The output goes LOW after time T of the mono shot.





In above image, the **first waveform shows a single pulse** where the signal is changing from 0 to 5v (low to high) and 5v to 0 (high to low) within a short period of time. **Second waveform shows a stream of 5-volt pulses** in the signal line. Now when some of the pulses in this pulse chain are failed to occur which are having the predefined interval time, a **Missing Pulse Detector Circuit** is required to detect those missing pulses. The detector circuit is capable to provide missing pulse notification. **Last waveform shown in the image is a missing pulse signal.**

Missing pulse generator circuit is an excellent application of the classic 555 timer IC. It can trigger an alarm or notify the user when there is some halt or interruption in some process.

1. Many electronics fan system provides continuous pulses during the operation. This circuit can easily determine and trigger the alarm if the fan has been stopped or not working as it should be.

2. In the medical field, the missing pulse detector circuit is used with heartbeat monitoring devices. This could alarm the doctors for abnormalities in the heartbeat.

3. This circuit is also very useful to detect a loss in alternating current supply.

4. It can also be used for half wave or full wave detection in various signal source measuring related operation.